

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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POWER BLOCK DIAGRAM

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MPC7447A DATA/NC PINS/BOOTBANGER

CPU PLL AND CONFIGURATION STRAPS

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INTREPID MEMORY INTERFACE/BOOTROM

DDR MEMORY MUXES

400PIN STACKED DDR SODIMM CONNECTOR

INTREPID AGP 4X/PCI

INTREPID ENET/FW/UATA/EIDE INTERFACES

INTREPID GPIOs/SERIAL/USB INTERFACES/SSCG

INTREPID POWER RAILS/1.5V LDO

INTREPID DECOUPLING

USB 2.0 INTERFACE (uPD720101)

CARDBUS INTERFACE (PCI1510)

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M11 POWER

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FIREWIRE PORTS

PMU

BATTERY CHARGER AND CONNECTOR

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CPU CORE VOLTAGE POWER SUPPLY

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SIGNAL CONSTRAINTS(PG1)-DDR MEM/CLK

SIGNAL CONSTRAINTS(PG2)-CPU

SIGNAL CONSTRAINTS(PG3)-DIGITAL/DIFF

SIGNAL CONSTRAINTS(PG4)-POWER NETS

FUNCTIONAL TESTPOINTS

REVISION HISTORY

SCHEMATIC CREF AND NETLIST REPORTS

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD  
DATE

ENG APPD  
DATE

A

356292

PRODUCTION RELEASED

12/17/04

?

SCHEM,MLB,PB15 "

12/17/2004

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EMI
GPU_SS	EXT_TMDS (BETTER/BEST)
VGA_BUFFER_RES	INT_TMDS (BEST128)
MMM	SUPERCAP
INT_TMDS (BETTER/BEST)	ADT7460
EXT_TMDS (BEST128)	
BACKUP_BATT	
ADT7467	

DIMENSIONS ARE IN MILLIMETERS


XX : \_\_\_\_\_

X.XX : \_\_\_\_\_

X.XXX : \_\_\_\_\_

ANGLES : \_\_\_\_\_

DO NOT SCALE DRAWING



THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD

DESIGNER


SCALE

SIZE

NONE

MATERIAL/FINISH NOTED AS APPLICABLE

D

 Apple Computer Inc.

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TITLE

SCHEM,MLB,PB15

DRAWING NUMBER

051-6680

REV.

A

SHT

1

OF

46

8

7

6

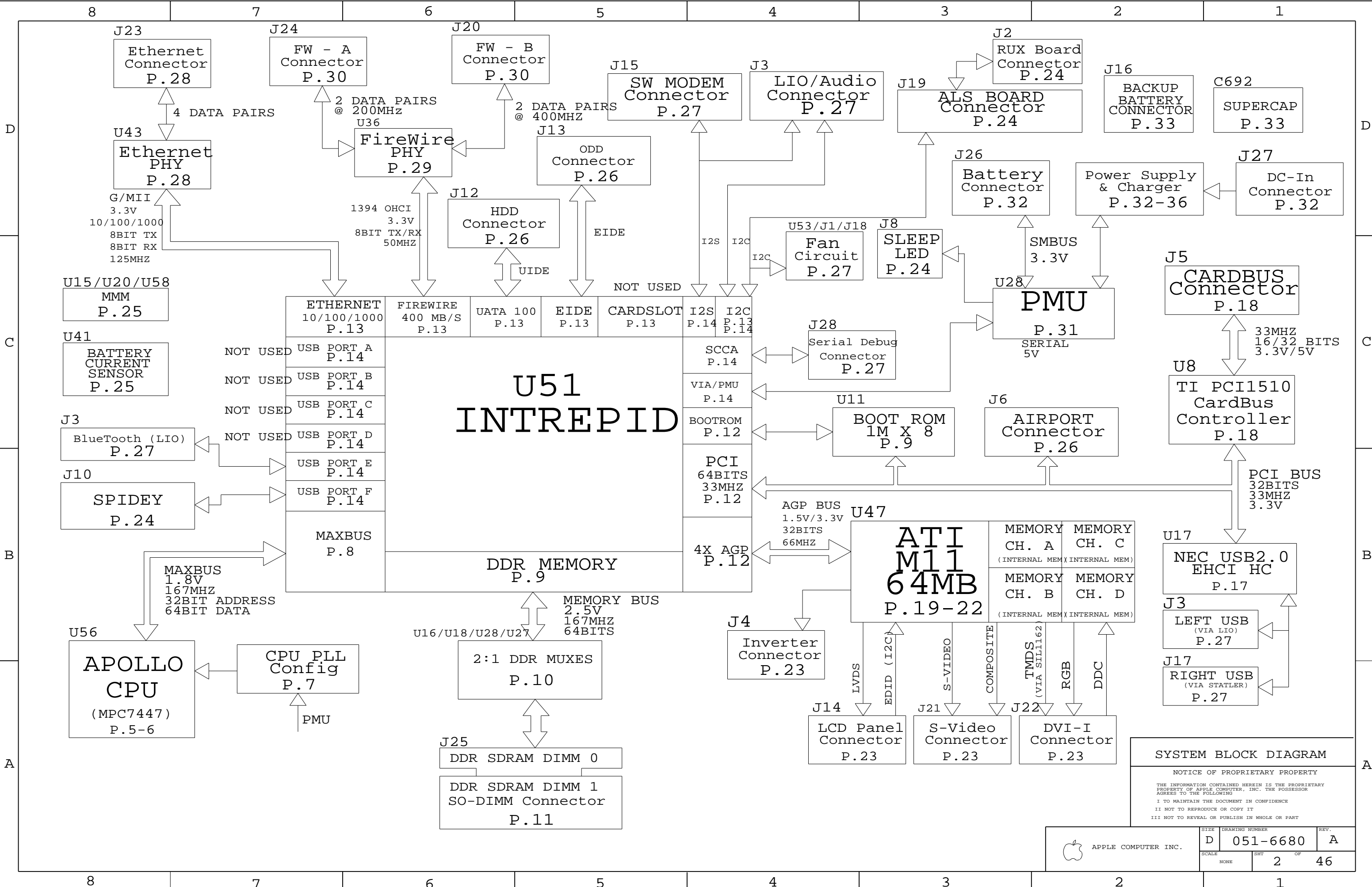
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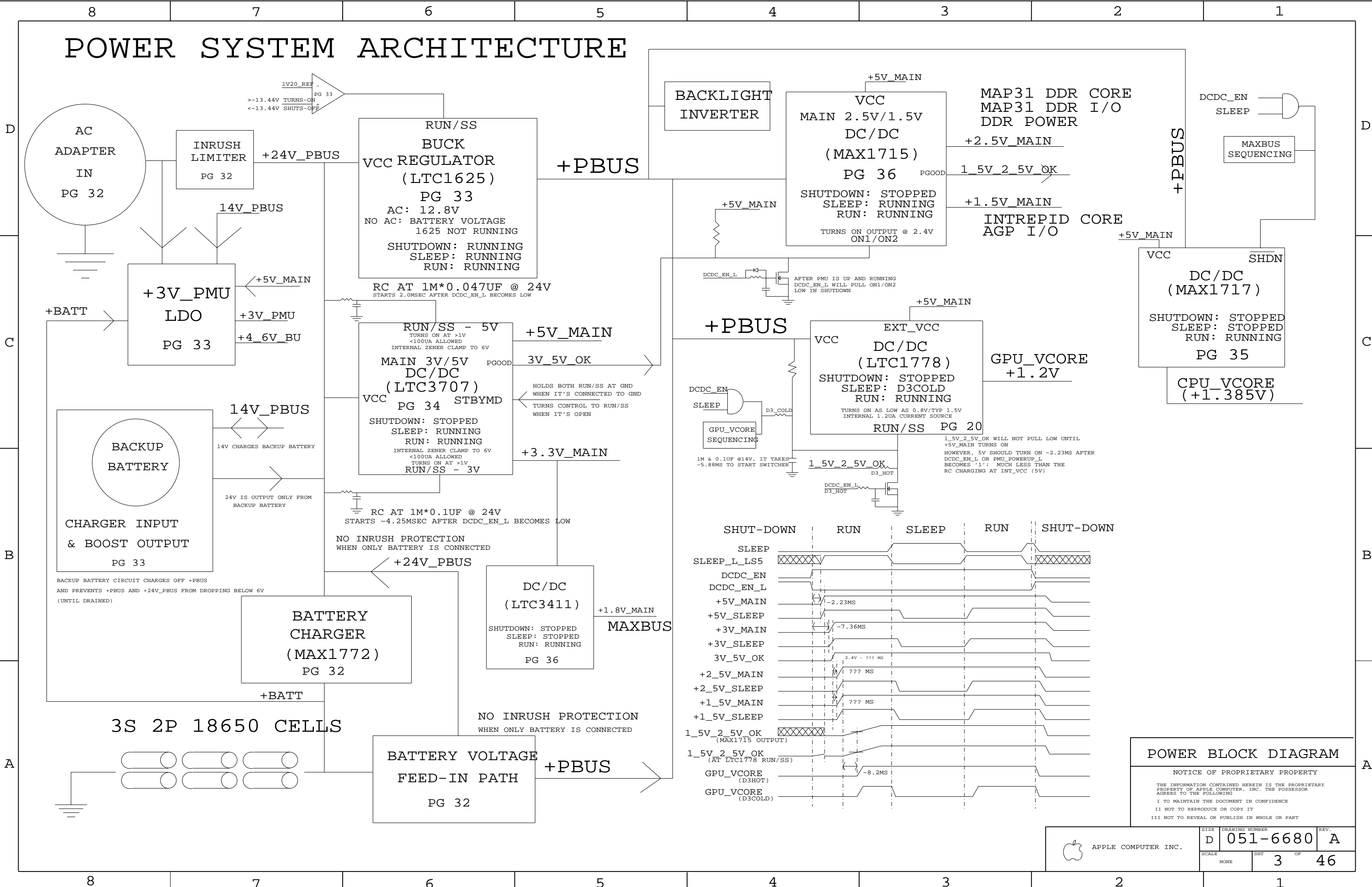
4

3

2

1





PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
1/2 OZ CU THICKNESS: 0.7 MILS  
1.0 OZ CU THICKNESS: 1.4 MILS

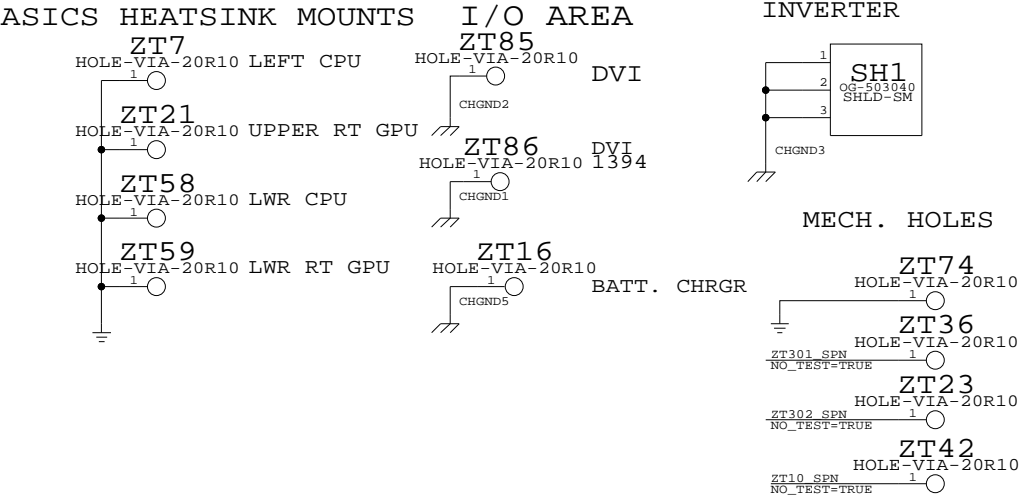
IMPEDANCE : 50 OHMS +/- 10%  
DIELECTRIC: FR-4  
LAYER COUNT: 10  
SIGNAL TRACE WIDTH: 4 MILS  
SIGNAL TRACE SPACING: 4 MILS  
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

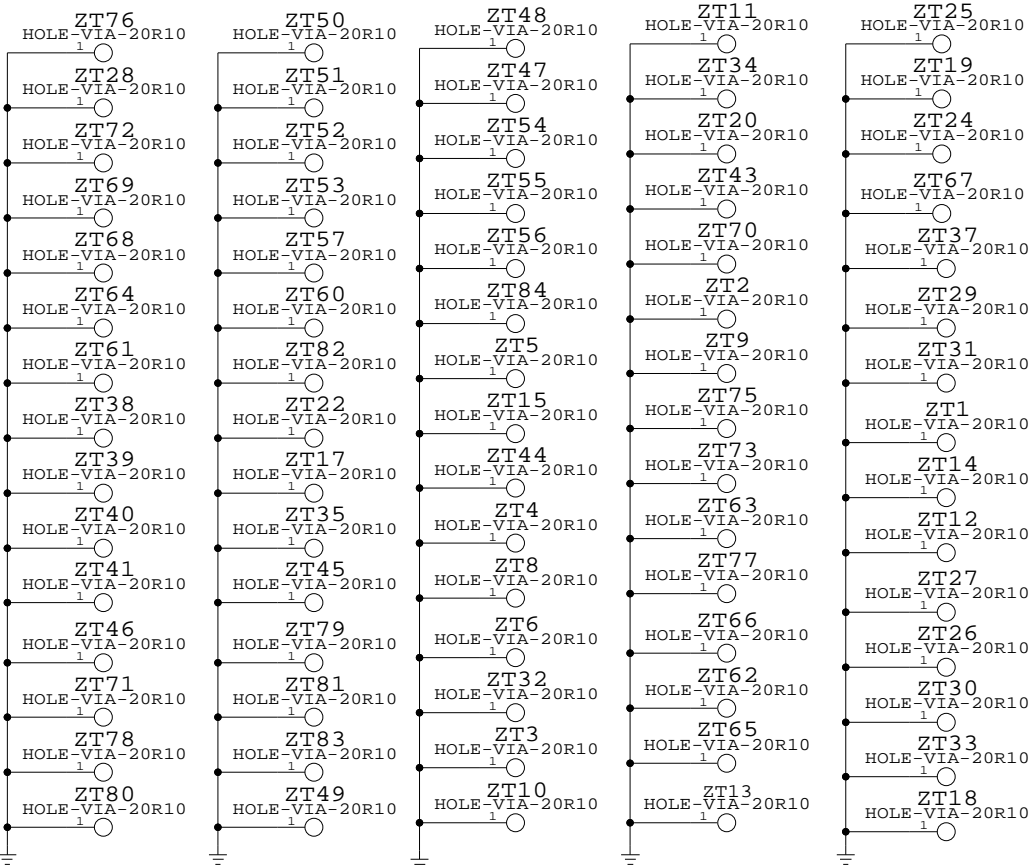
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA				SIGNAL (1/2 OZ + COPPER PLATING)	
1				SIGNAL (1/2 OZ)	
2	PREPREG (3 MIL)			GROUND (1/2 OZ)	
3	PREPREG (3 MIL)			SIGNAL (1/2 OZ)	
4	CORE (3 MIL)			CUT POWER PLANE (1 OZ)	
5	PREPREG (5 MIL)			CUT POWER PLANE (1 OZ)	
6	CORE (5 MIL)			SIGNAL (1/2 OZ)	
7	PREPREG (5 MIL)			GROUND (1/2 OZ)	
8	CORE (3 MIL)			SIGNAL (1/2 OZ)	
9	PREPREG (3 MIL)			SIGNAL (1/2 OZ + COPPER PLATING)	
10	PREPREG (3 MIL)				

BOARD HOLES  
CHASSIS MOUNTS



GROUND VIAS



BOARD INFORMATION

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SIZE	D	DRAWING NUMBER	051-6680	REV.	A
SCALE	NONE	SHT	4	OF	46





8	7	6	5	4	3	2	1
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2

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1



D C B

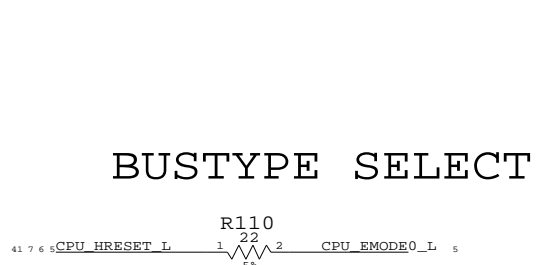
## B

## B



A

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION
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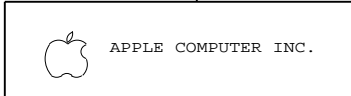
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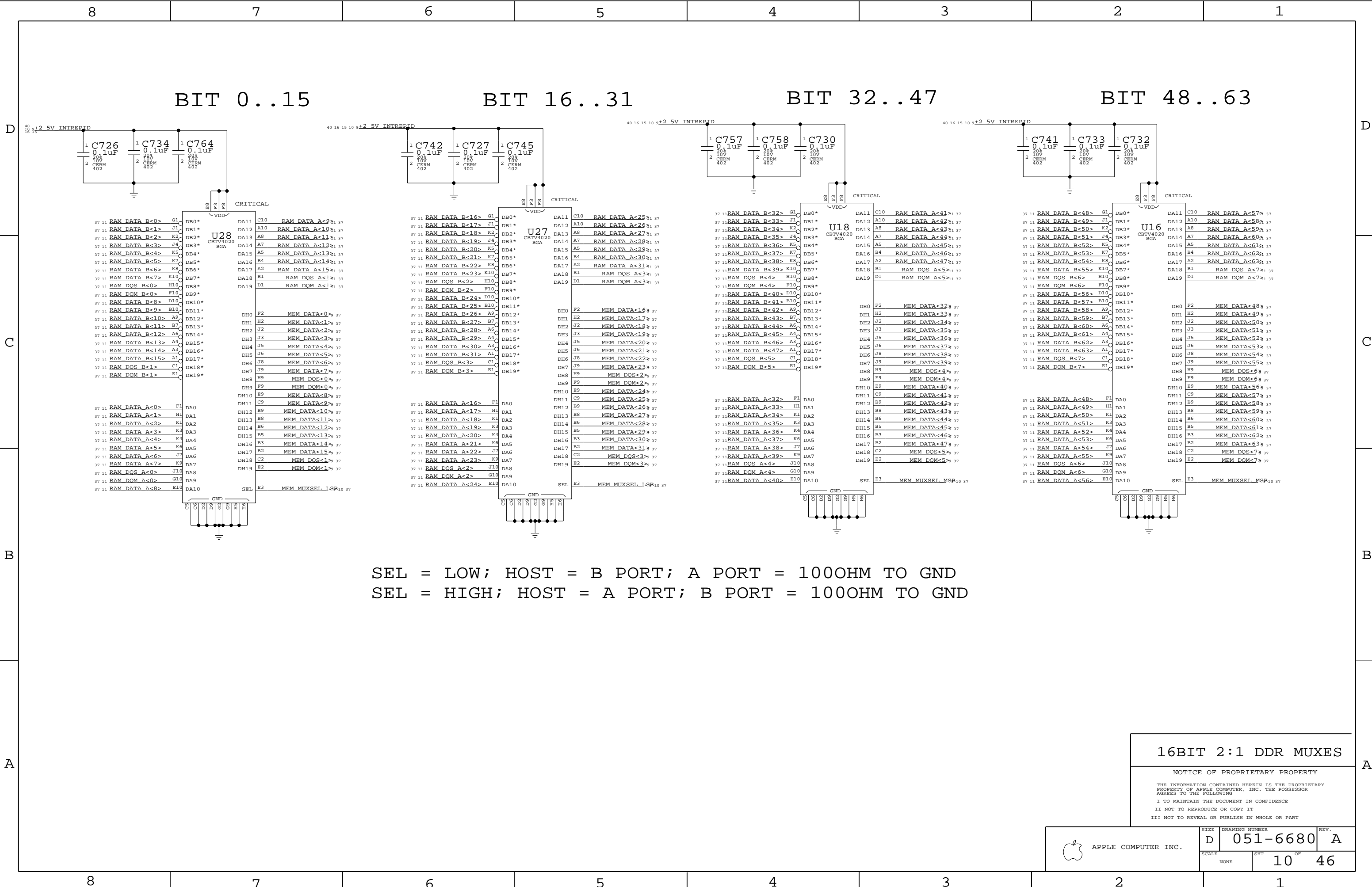
SIZE	DRAWING NUMBER	REV.
D	051-6680	A

SCALE	SHT	OF
NONE	7	46









SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND  
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

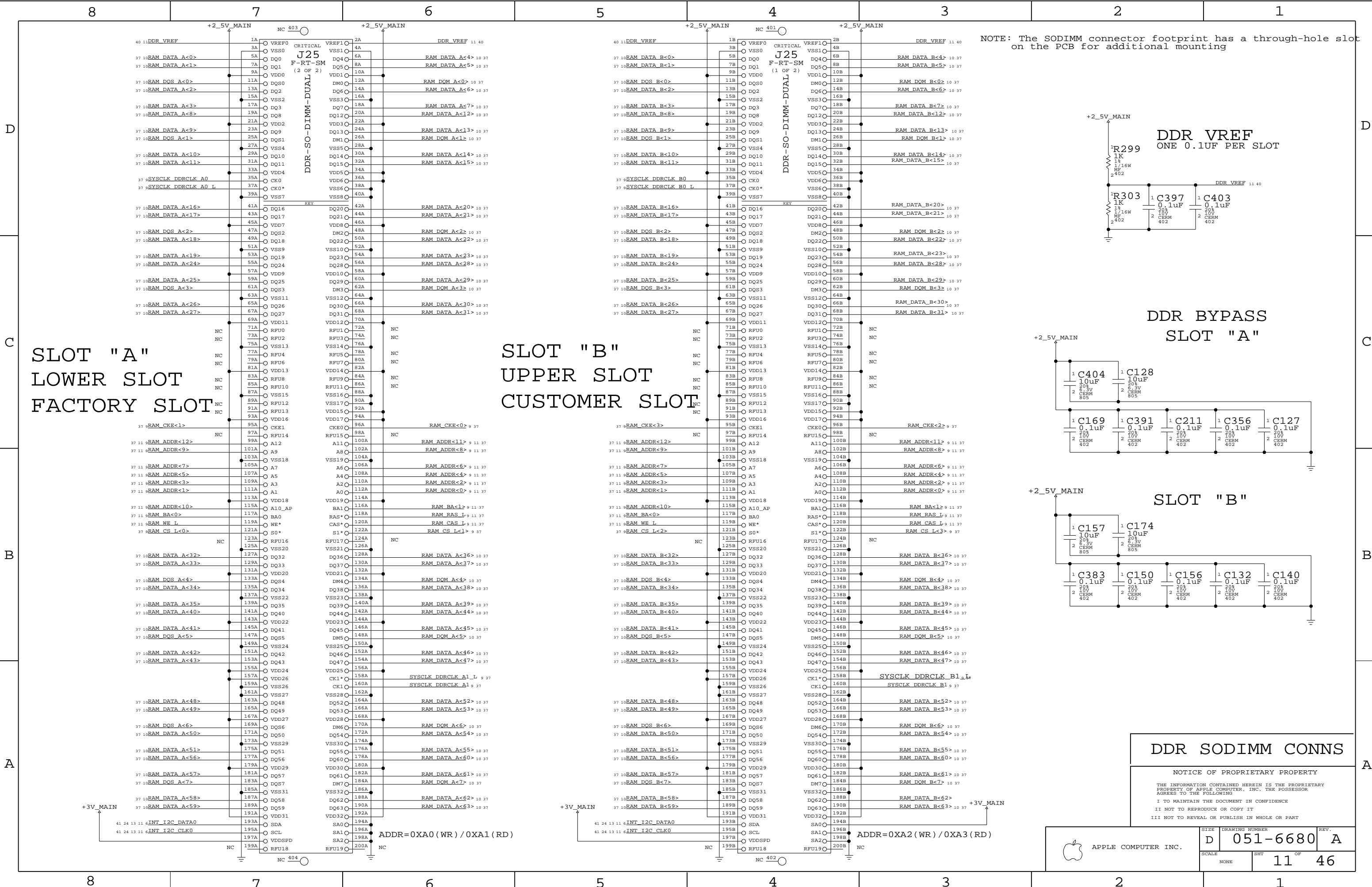
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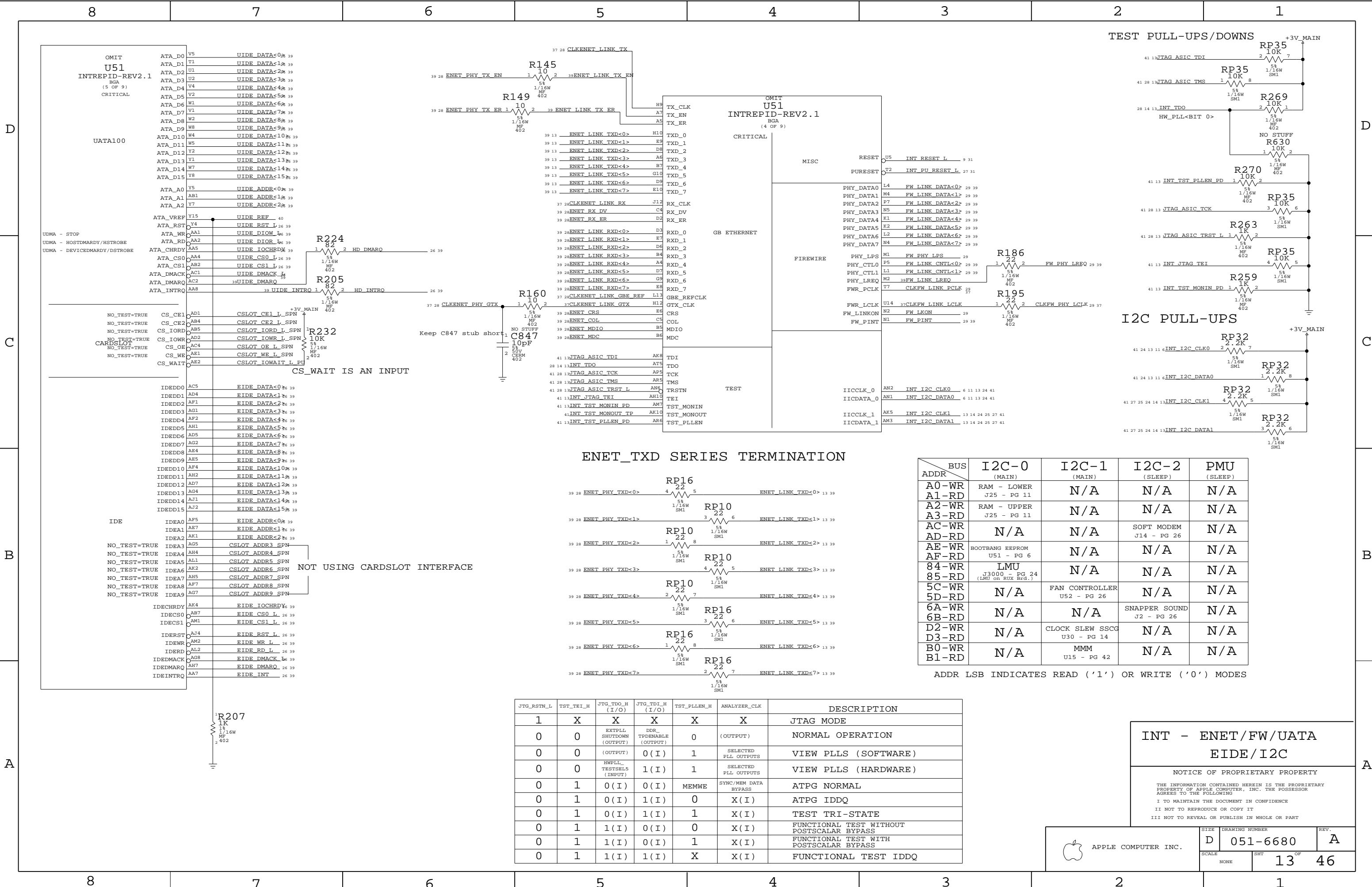


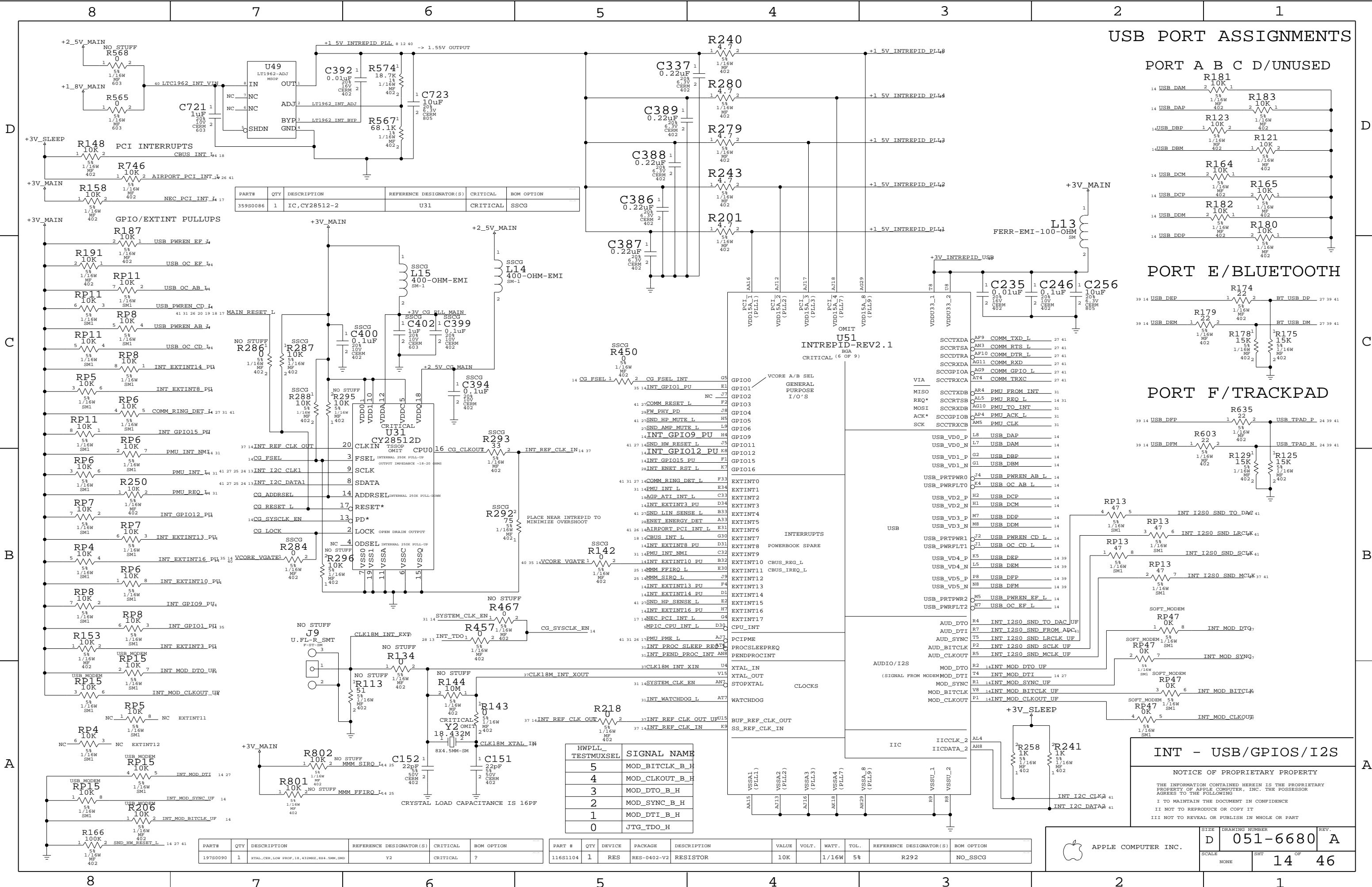
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NONE	10	46



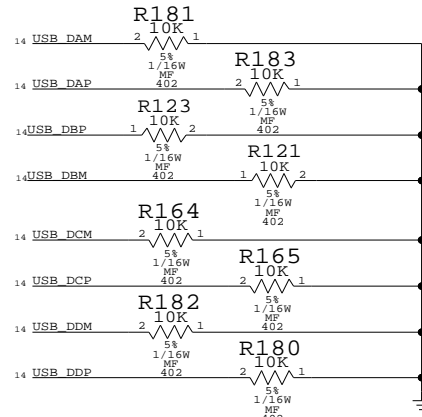




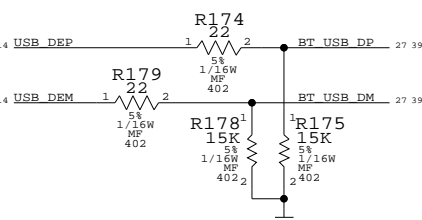


USB PORT ASSIGNMENTS

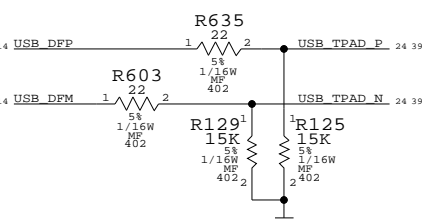
PORT A B C D/UNUSED



PORT E/BLEETOOTH



PORT F/TRACKPAD



INT - USB/GPIOS/I2S


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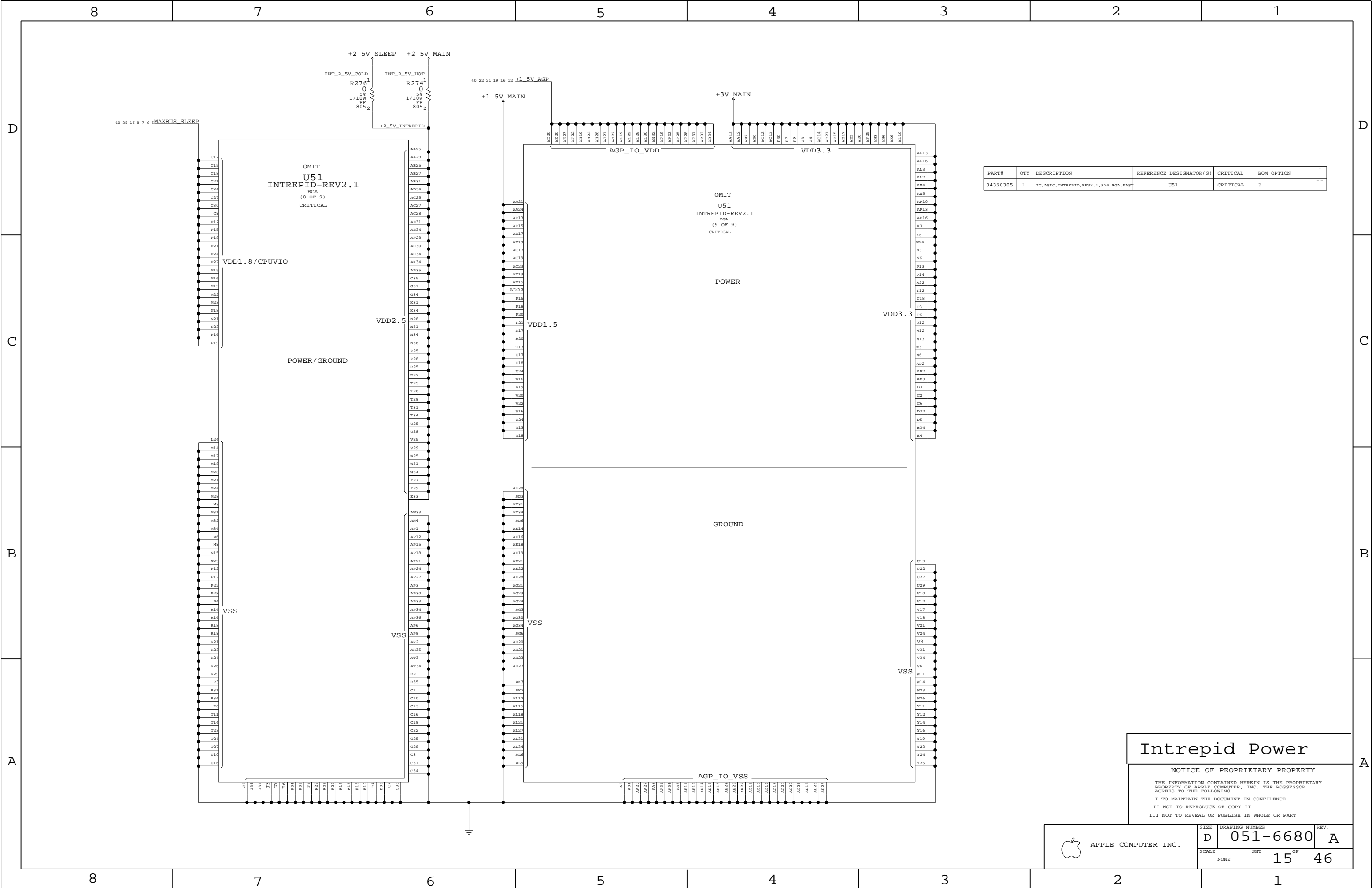
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

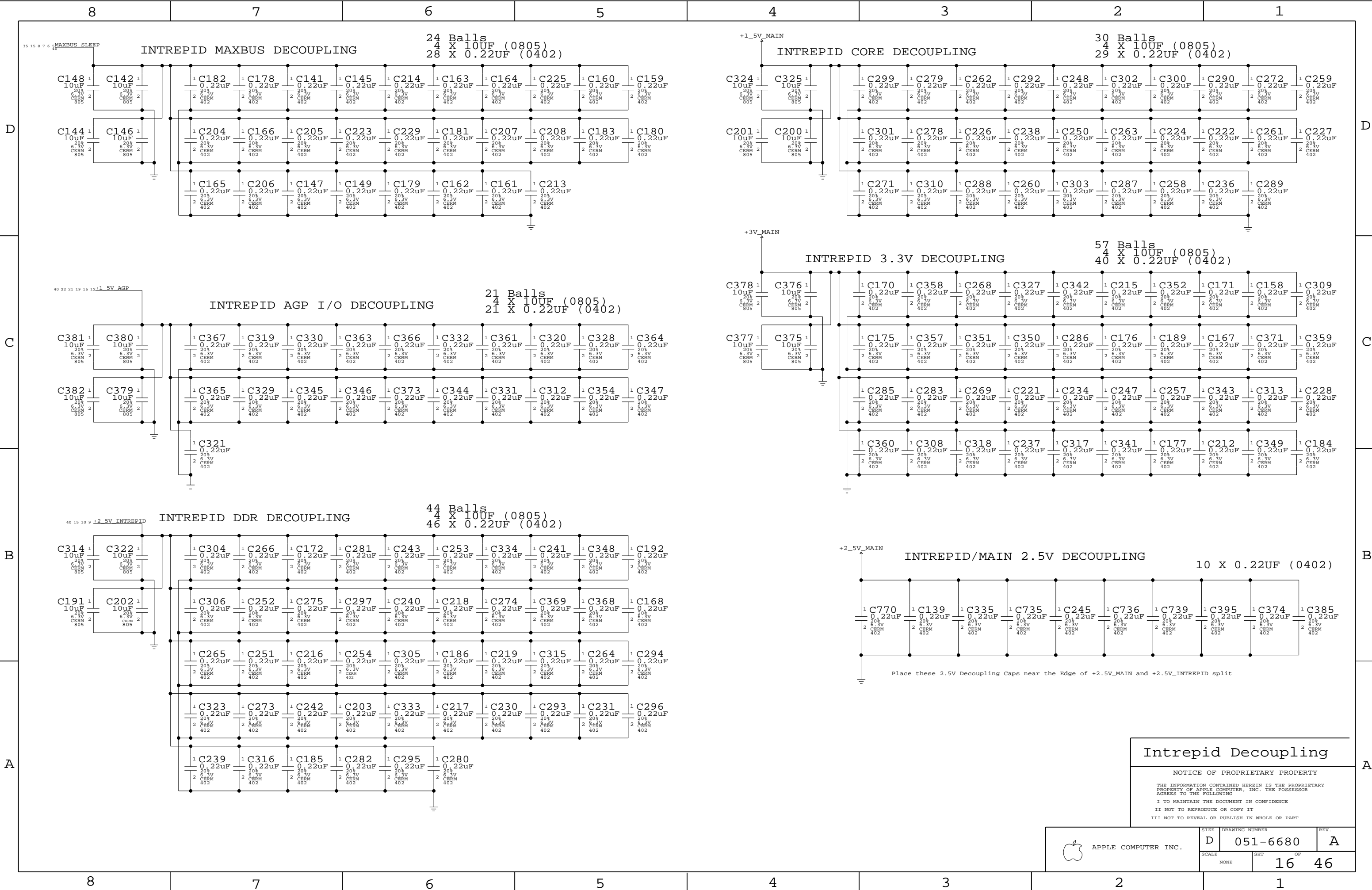
HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

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SIZE	D	DRAWING NUMBER	051-6680	REV.	A
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Intrepid Decoupling

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SIZE

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051-6680

REV.

A

SCALE

NONE

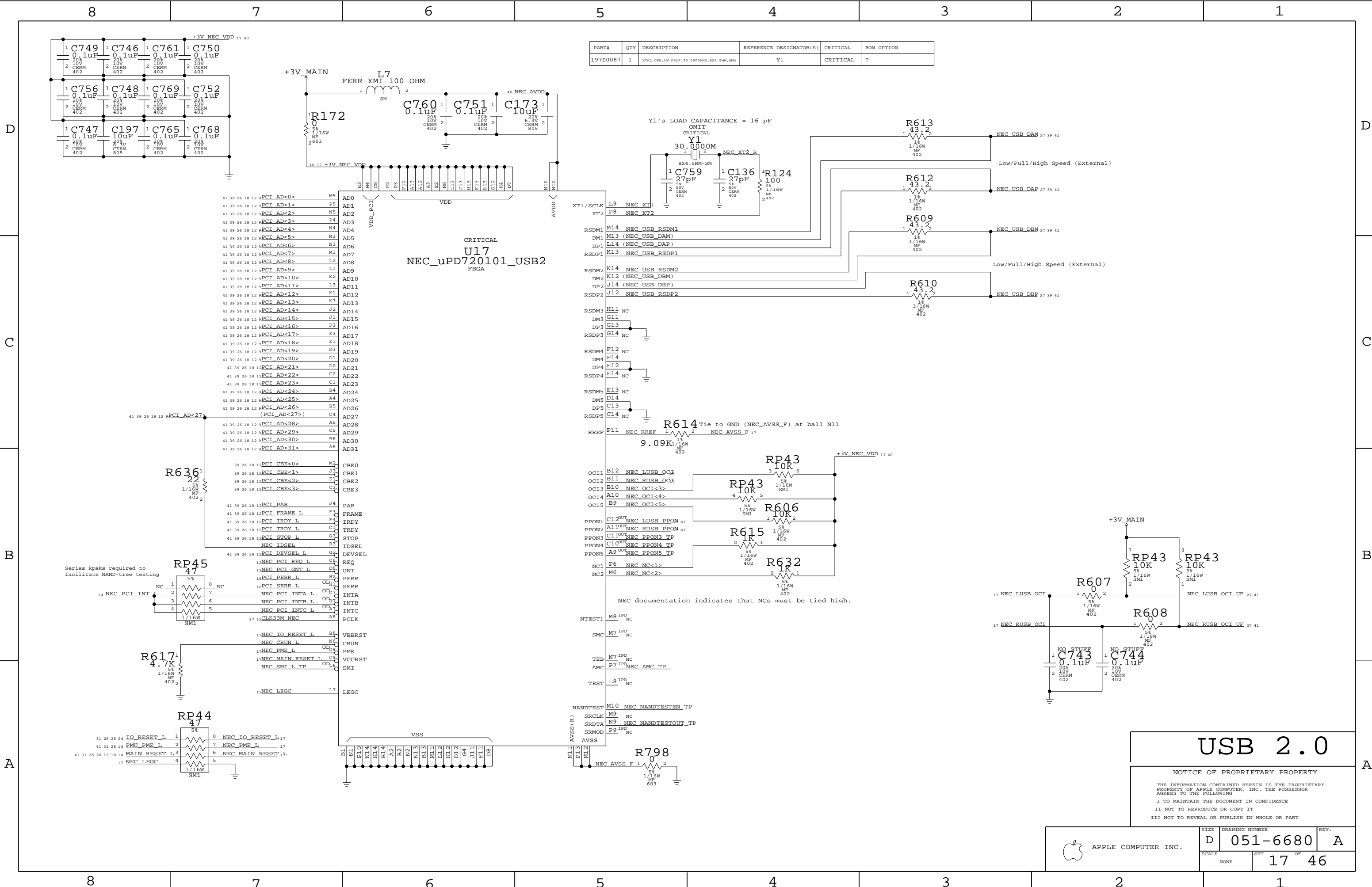
SHT

OF

16

46





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL, CER, 16 MHZ, 30.0000MHZ, 8X4.5MM, SMD	Y1	CRITICAL	?

USB 2.0

NOTICE OF PROPRIETARY PROPERTY

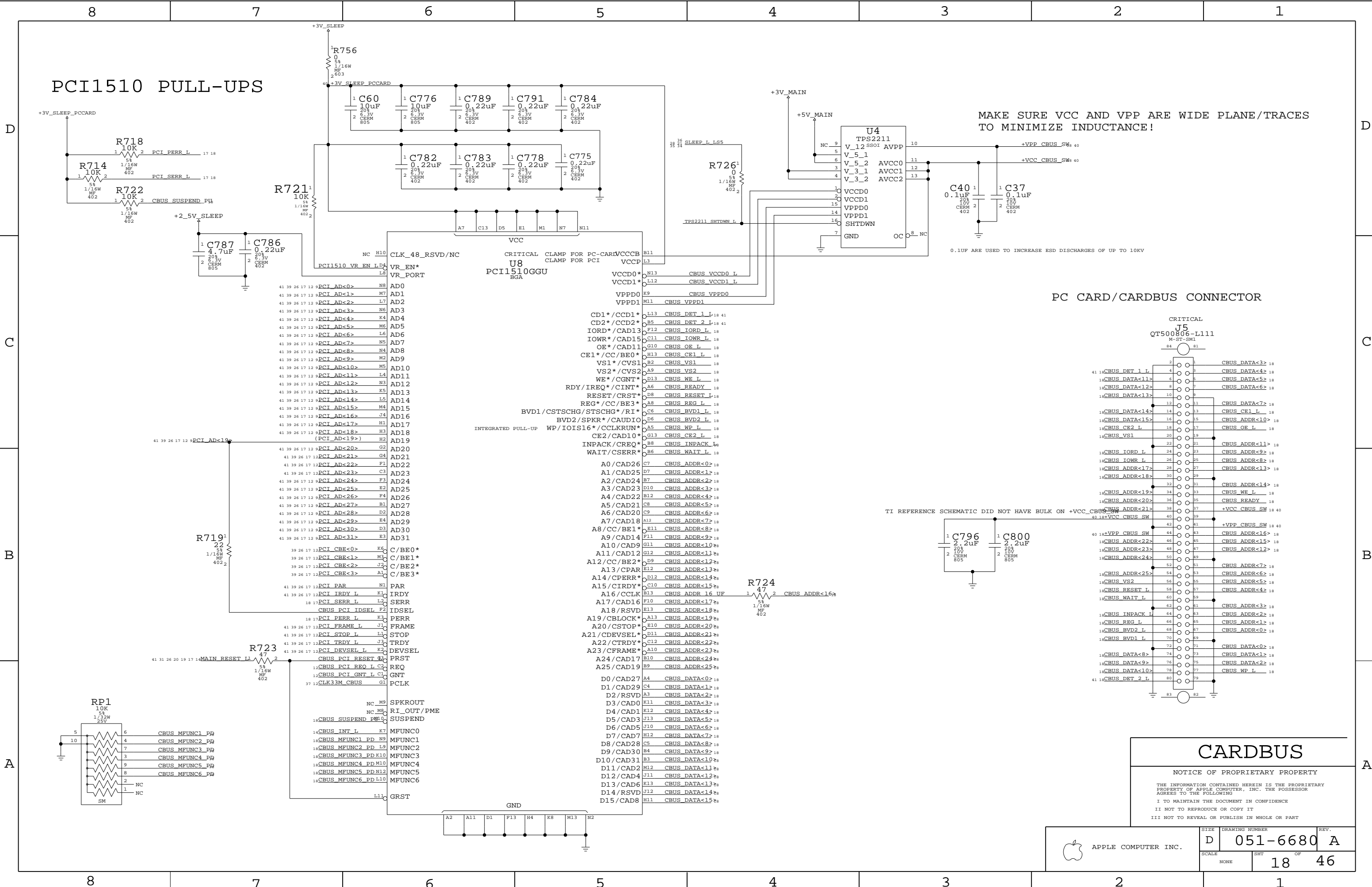
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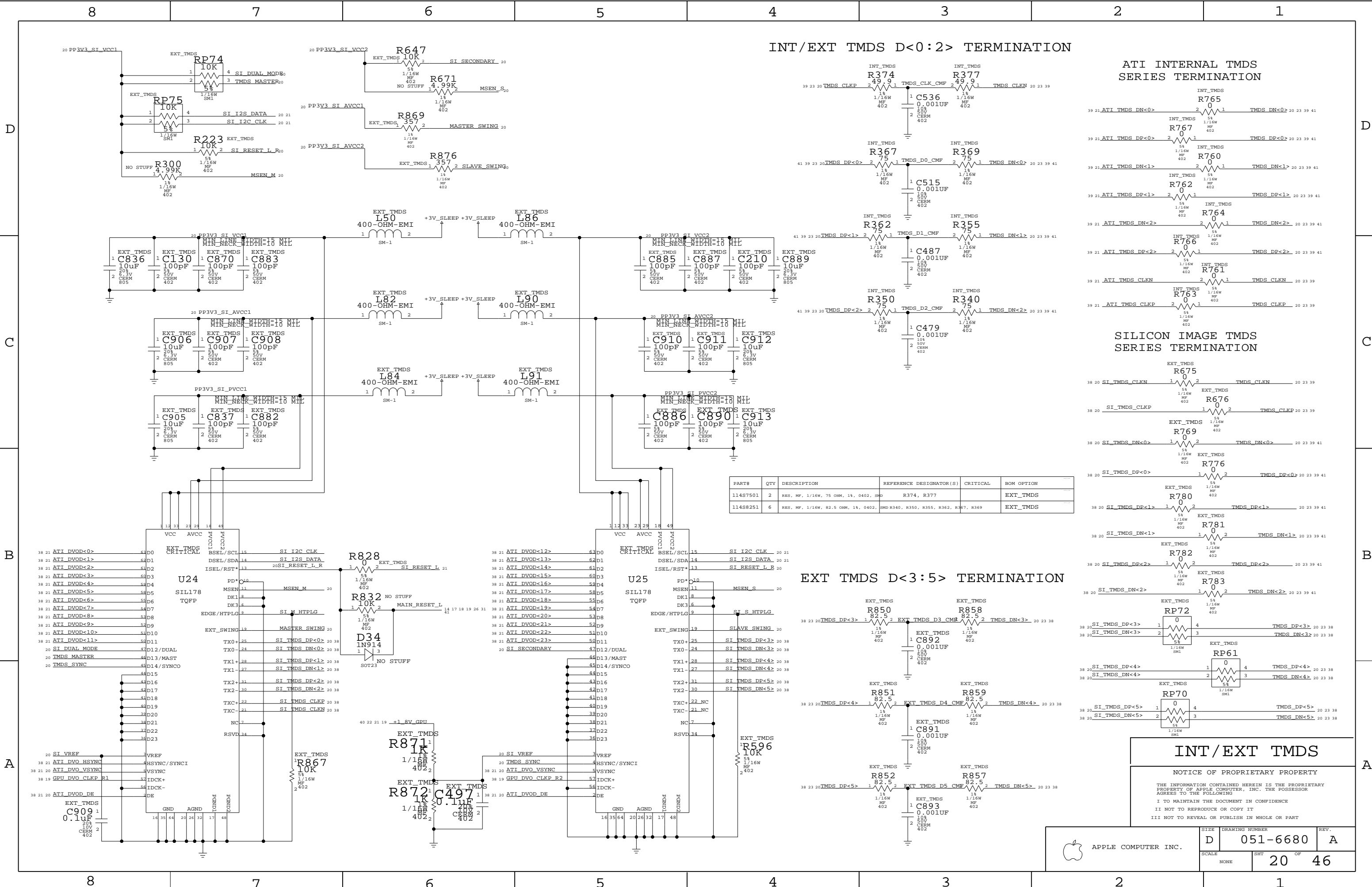
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6680	A
SCALE	NONE		SHT
	17		OF 46







INT/EXT TMSD D<0:2> TERMINATION

ATI INTERNAL TMSD SERIES TERMINATION

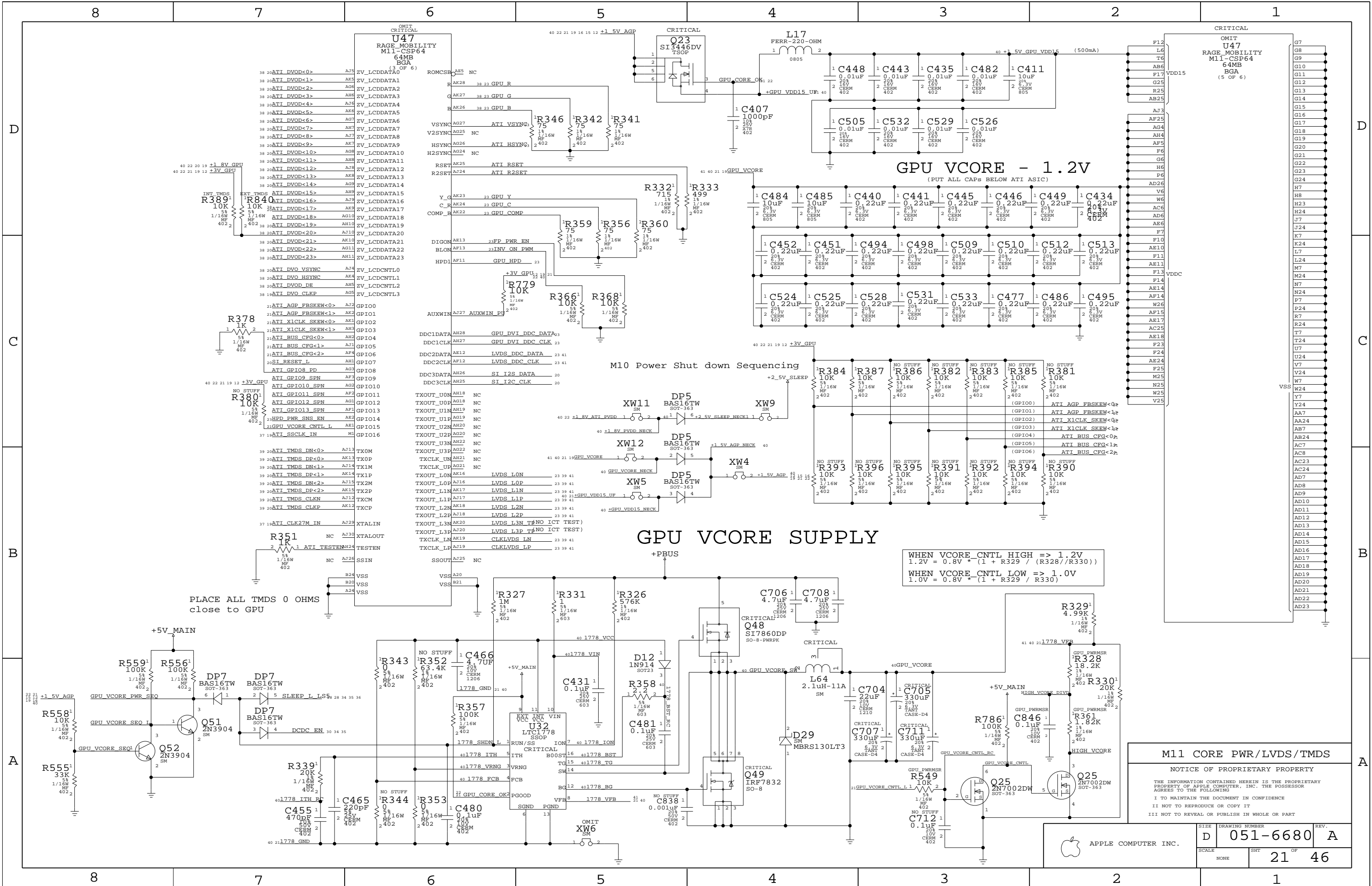
SILICON IMAGE TMSD SERIES TERMINATION

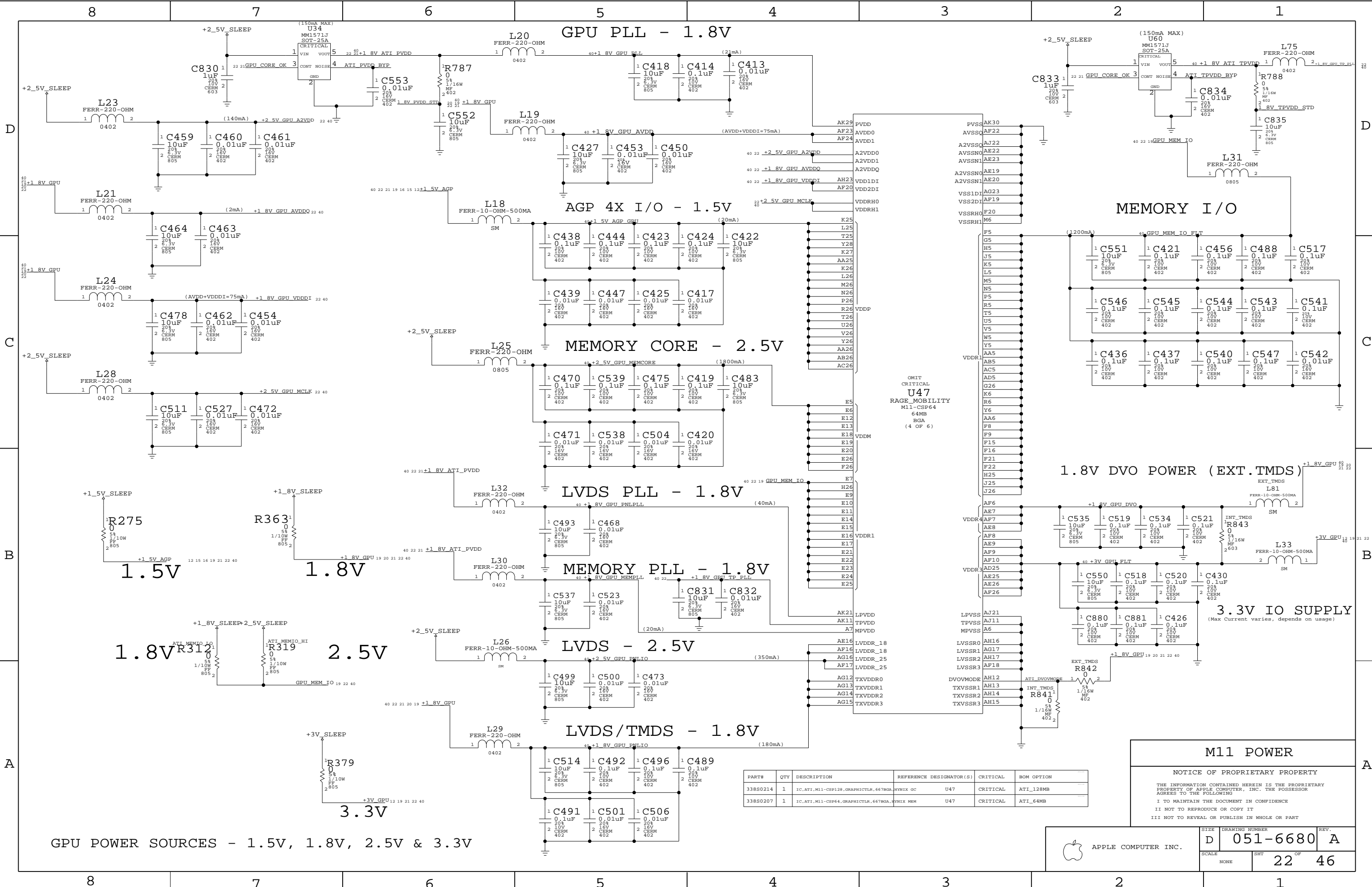
EXT TMSD D<3:5> TERMINATION

INT/EXT TMSD

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CS128,GRAPHICCTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICCTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

M11 POWER

NOTICE OF PROPRIETARY PROPERTY

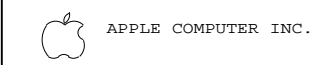
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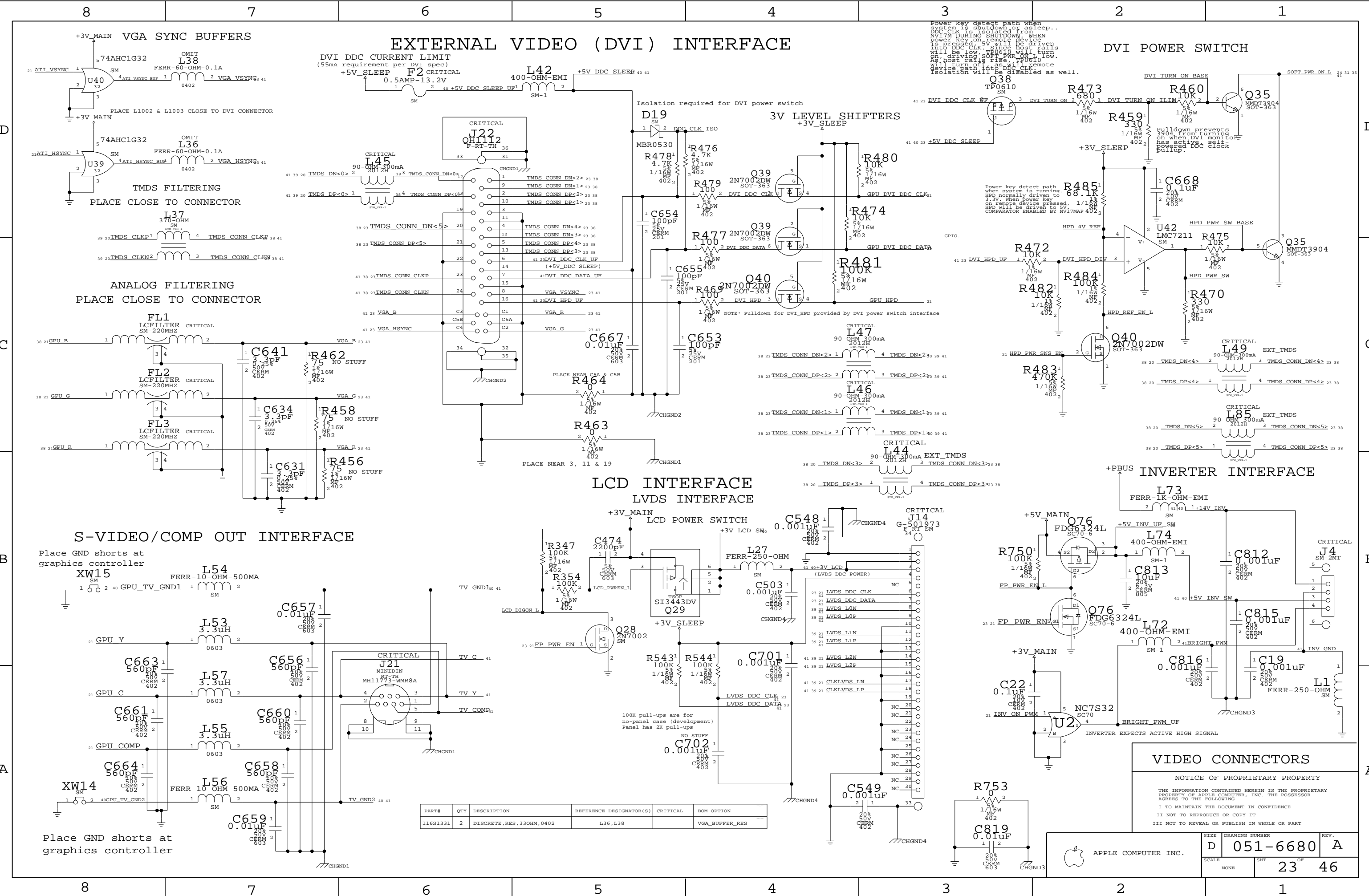
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

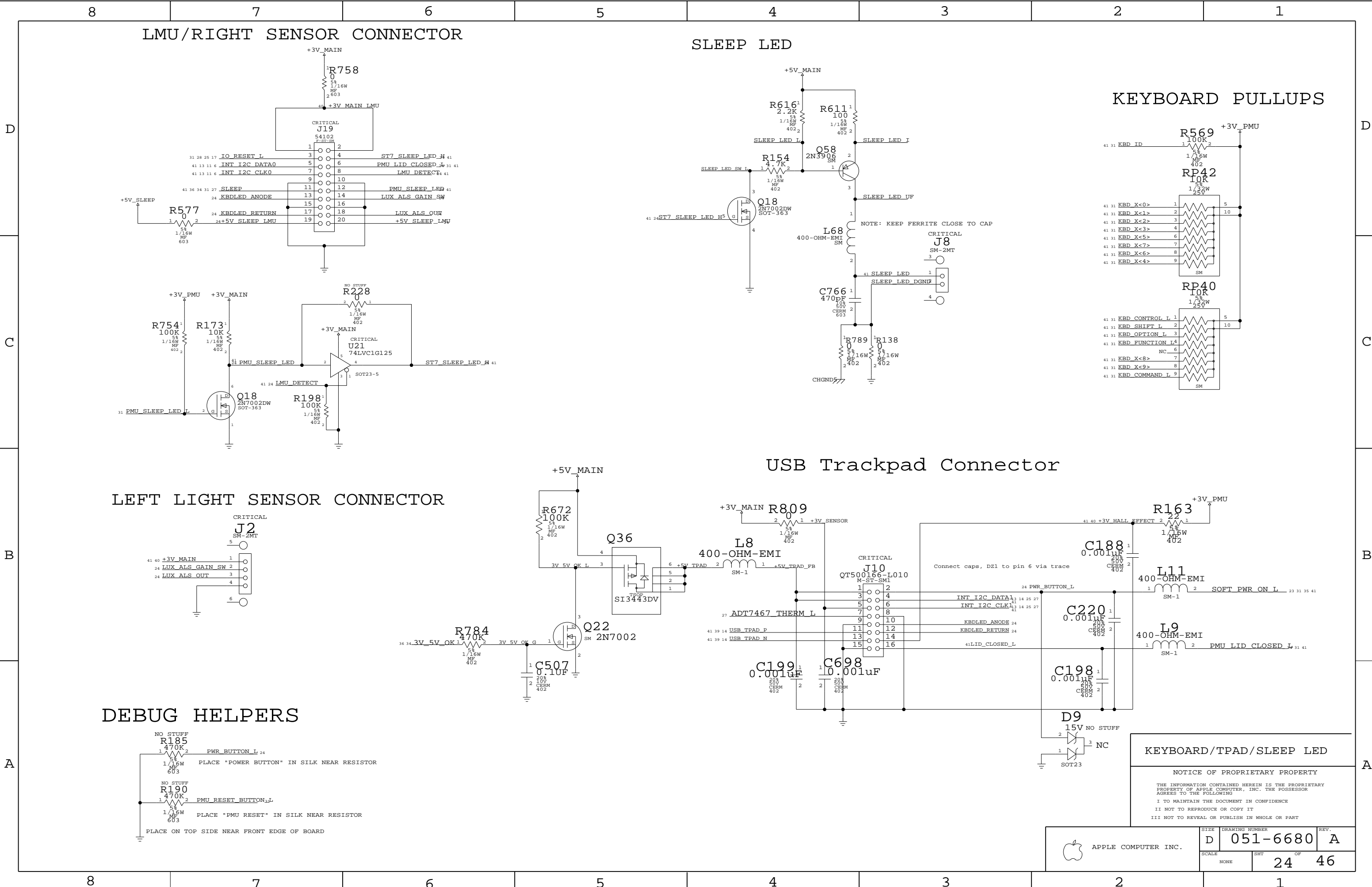
II NOT TO REPRODUCE OR COPY IT

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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
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NONE		







LMU/RIGHT SENSOR CONNECTOR

SLEEP LED

KEYBOARD PULLUPS

LEFT LIGHT SENSOR CONNECTOR

USB Trackpad Connector

DEBUG HELPERS

KEYBOARD/TPAD/SLEEP LED

NOTICE OF PROPRIETARY PROPERTY

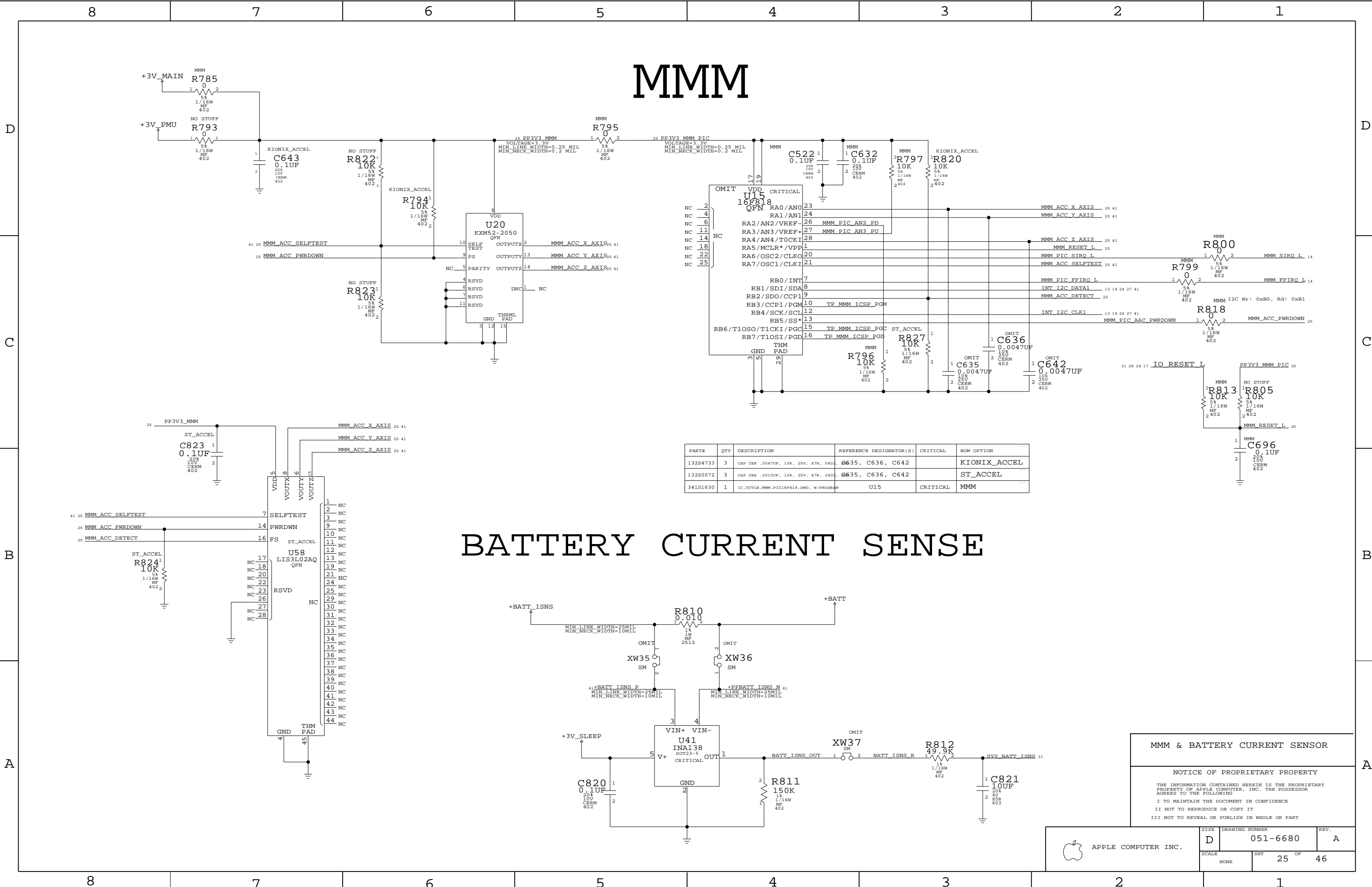
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SIZE	DRAWING NUMBER	REV.
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NONE	24	46





MMM

BATTERY CURRENT SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S4733	3	CAP CER .0047UF, 10%, 25V, X7R, 0402	C635, C636, C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402	C635, C636, C642		ST_ACCEL
341S1630	1	IC, UCTLA, MMM, PIC16F818, SMD, W/PROGRAM	U15	CRITICAL	MMM

MMM & BATTERY CURRENT SENSOR

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APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-6680

REV. A

SCALE NONE

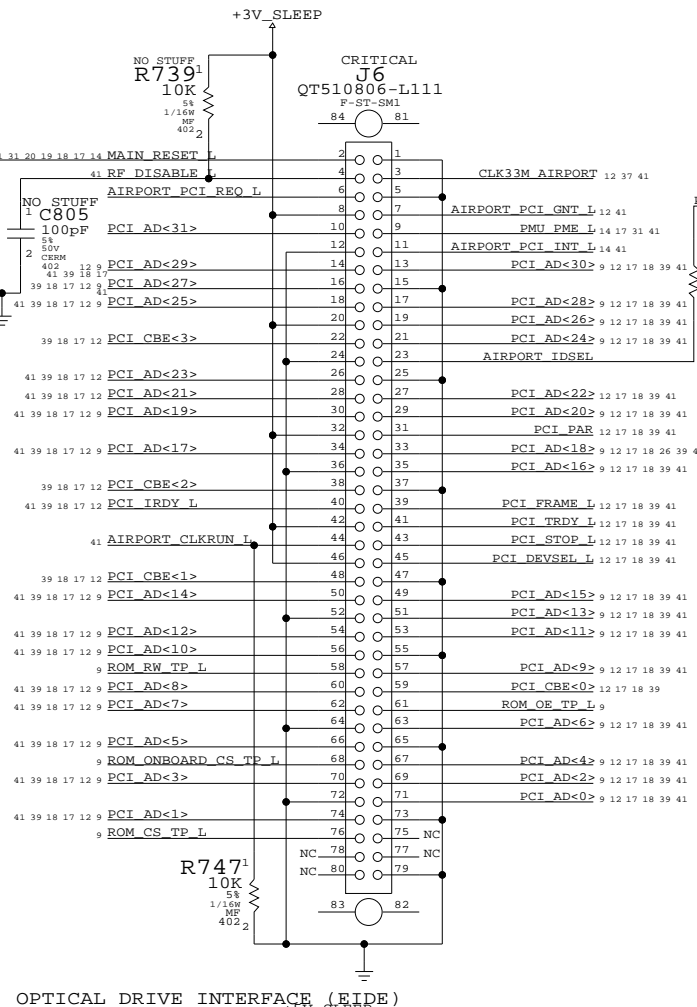
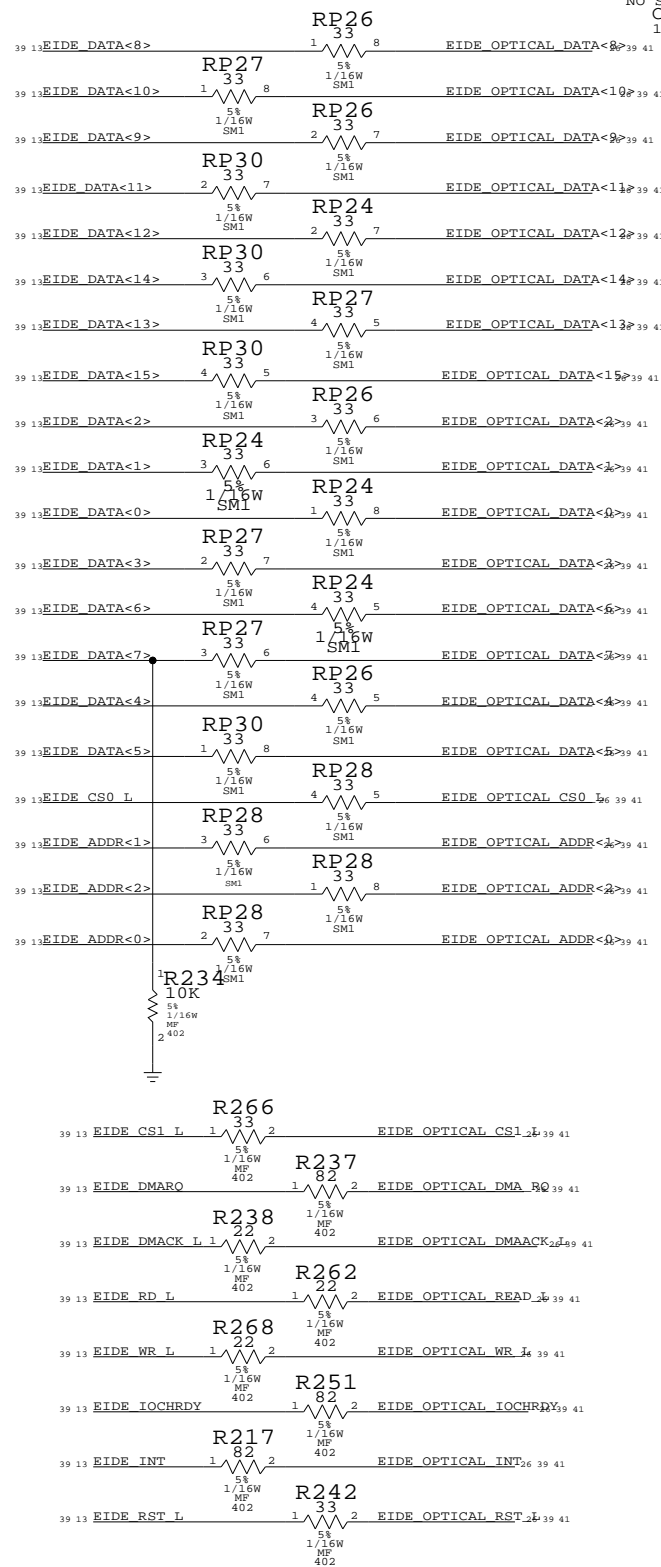
SHT 25

OF 46

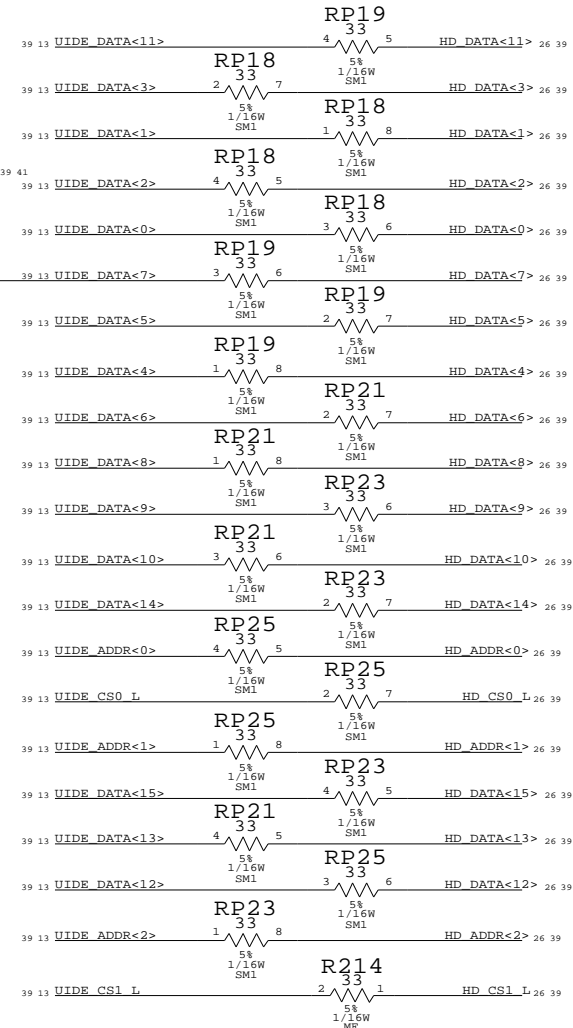
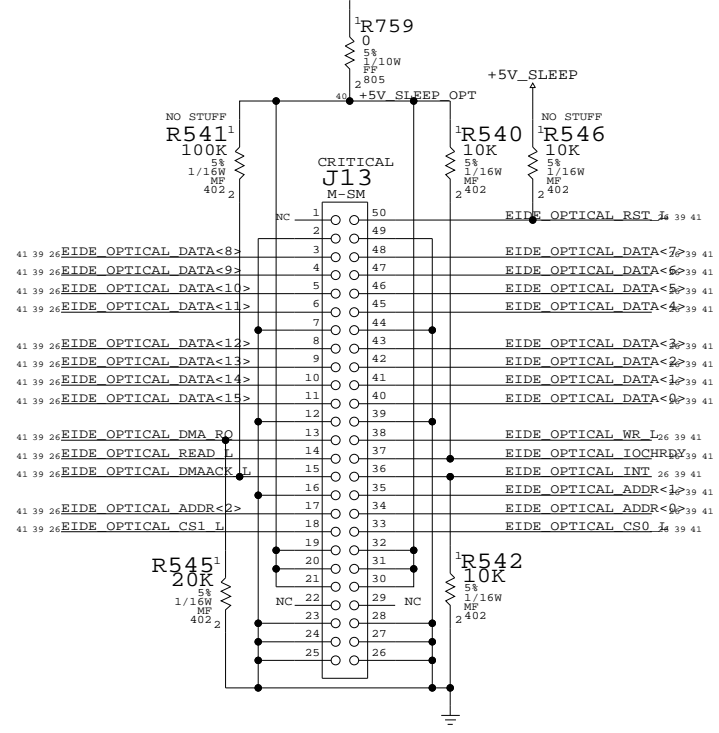
## WIRELESS INTERFACE

## HARD DRIVE INTERFACE (UATA100)

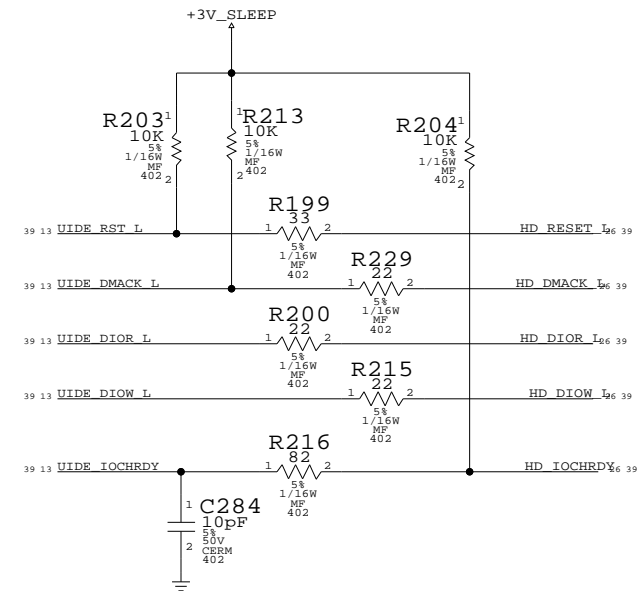
PLACE SERIES R CLOSE TO INTERPID



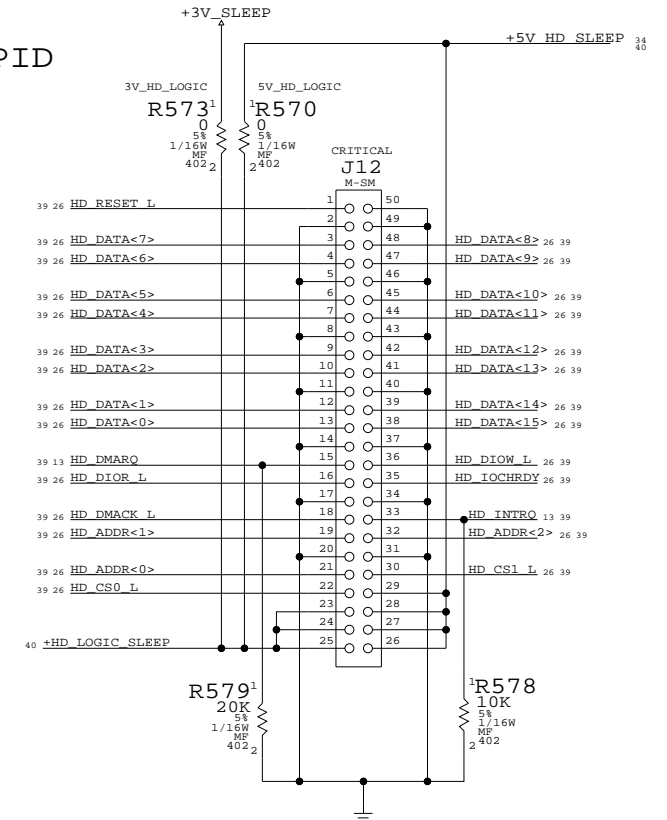
OPTICAL DRIVE INTERFACE (EIDE) <sup>+5V SLEEP</sup>



PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN  
+5V\_HD\_SLEEP AND +3V\_SLEEP

## INTERNAL I/O CONNECTORS


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LEFT I/O & AUDIO BOARD (LIO)

RIGHT USB BOARD

SOFT MODEM CONN

SERIAL DEBUG INTERFACE

FAN INTERFACE  
FAN CONTROLLER

CPU FAN

GPU FAN

FAN/MODEM/SOUND/BACKUP BATT.

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SIZE	DRAWING NUMBER	REV.
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NONE	27	46

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D

C

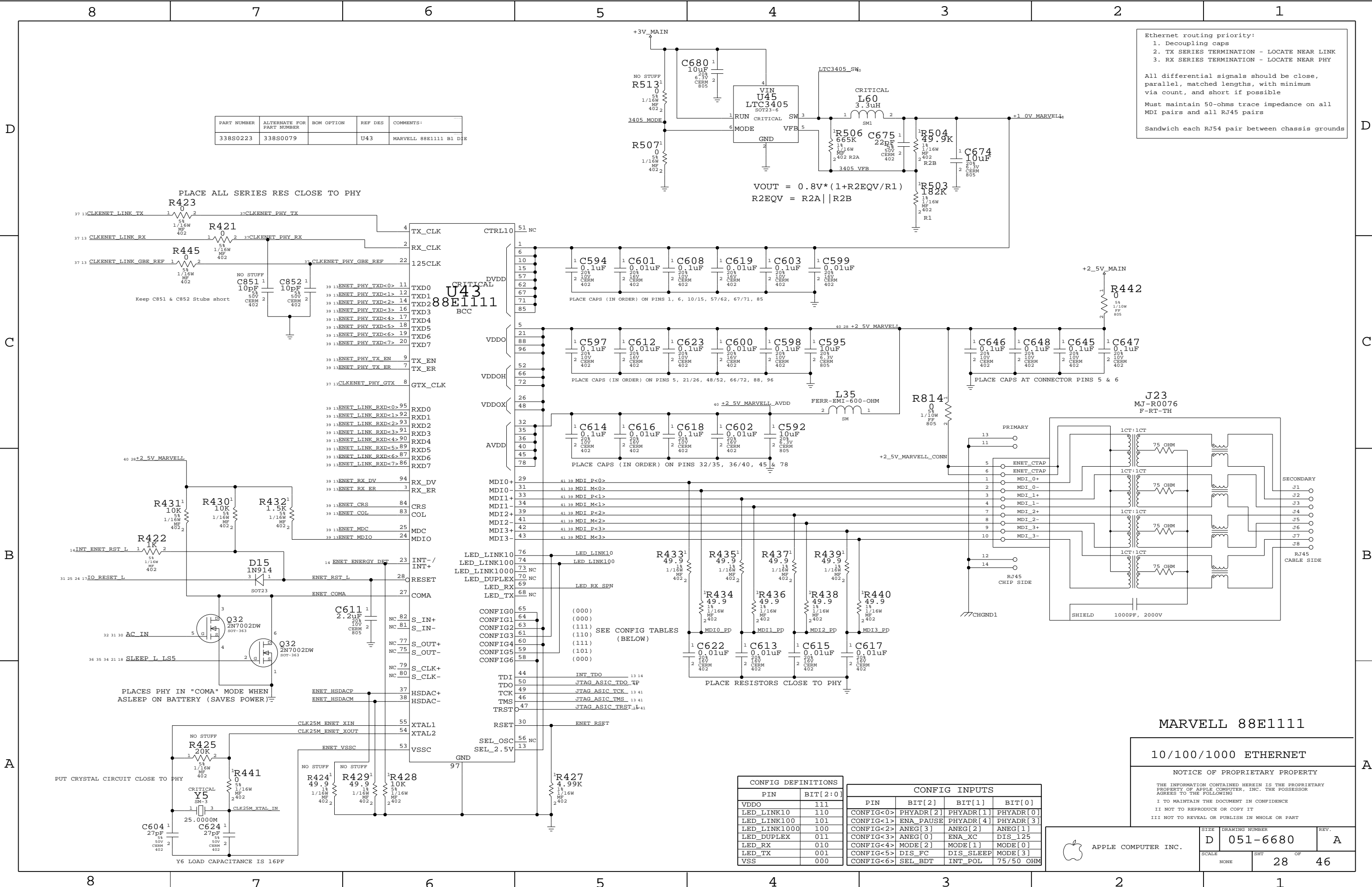
C

B

B

A

A



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079		U43	MARVELL 88E1111 B1 DIE

Ethernet routing priority:  
1. Decoupling caps  
2. TX SERIES TERMINATION - LOCATE NEAR LINK  
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

MARVELL 88E1111

10/100/1000 ETHERNET

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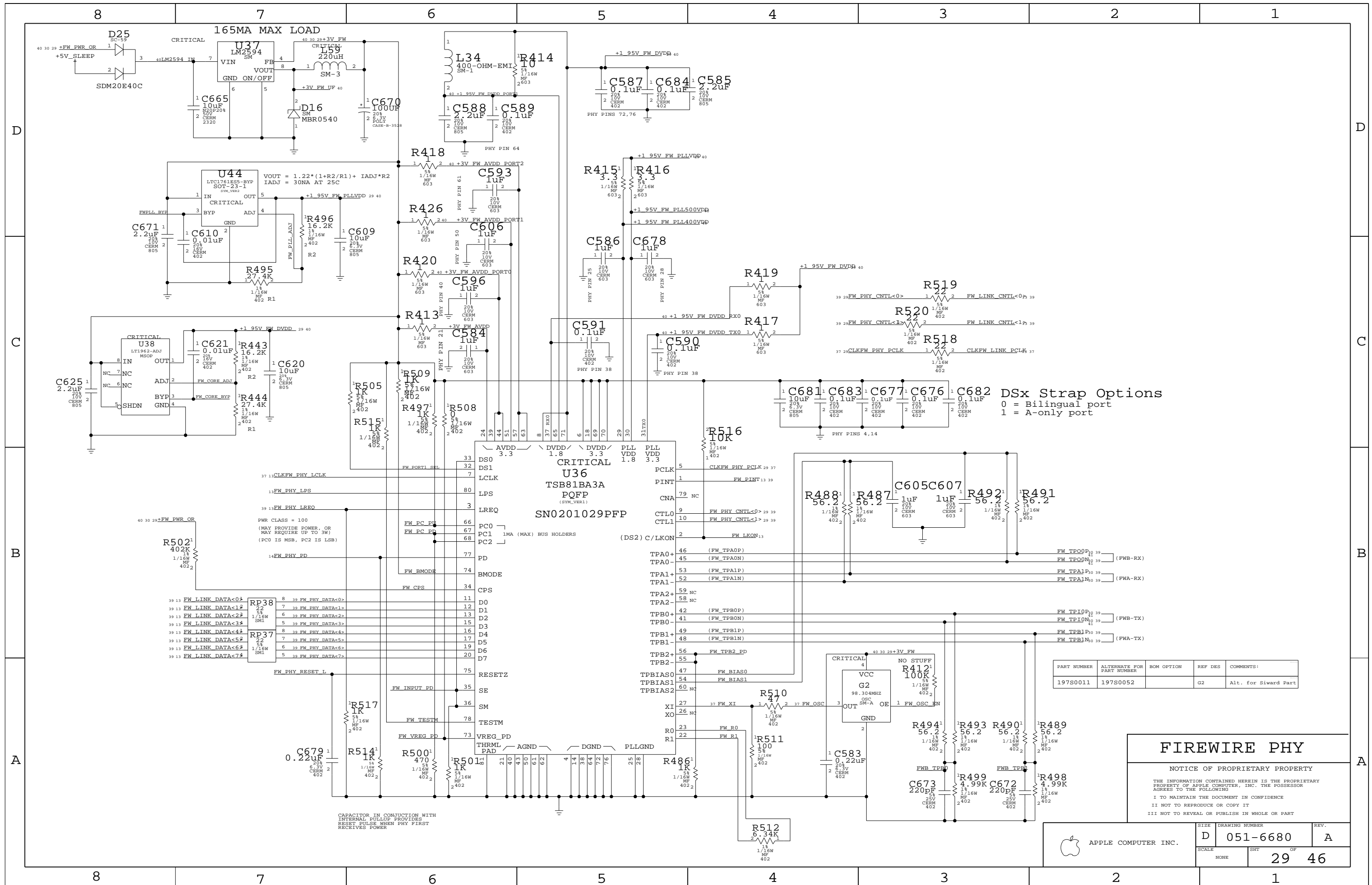


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE	SHT	OF
NONE	28	46

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM



PORT POWER SWITCH

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0  
1394a/b  
(BILINGUAL)  
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)  
BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

PORT 1  
1394a ONLY  
514-0057

FIREWIRE PORTS

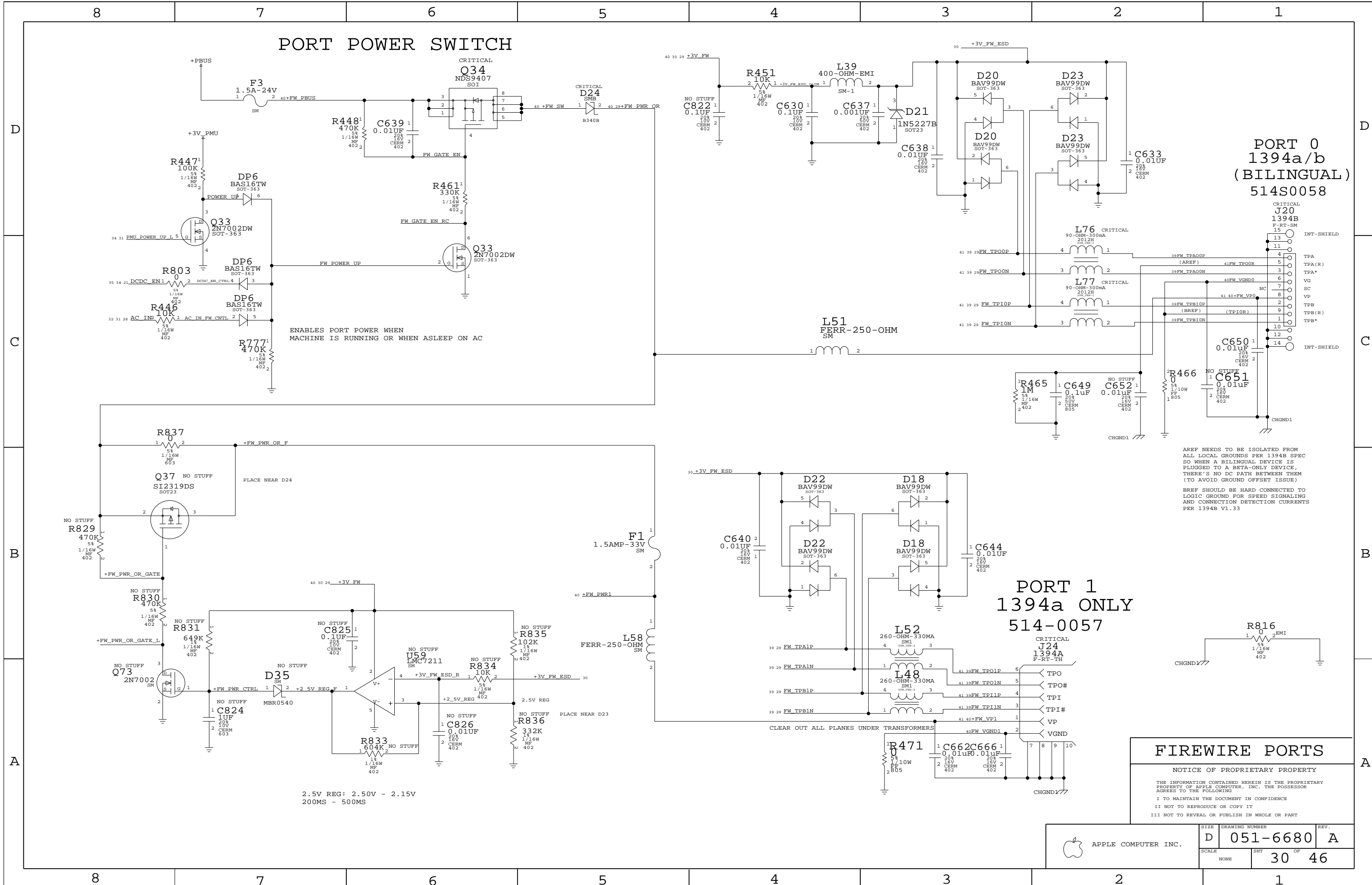
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE	SHT	OF
NONE	30	46





# DC POWER INPUT

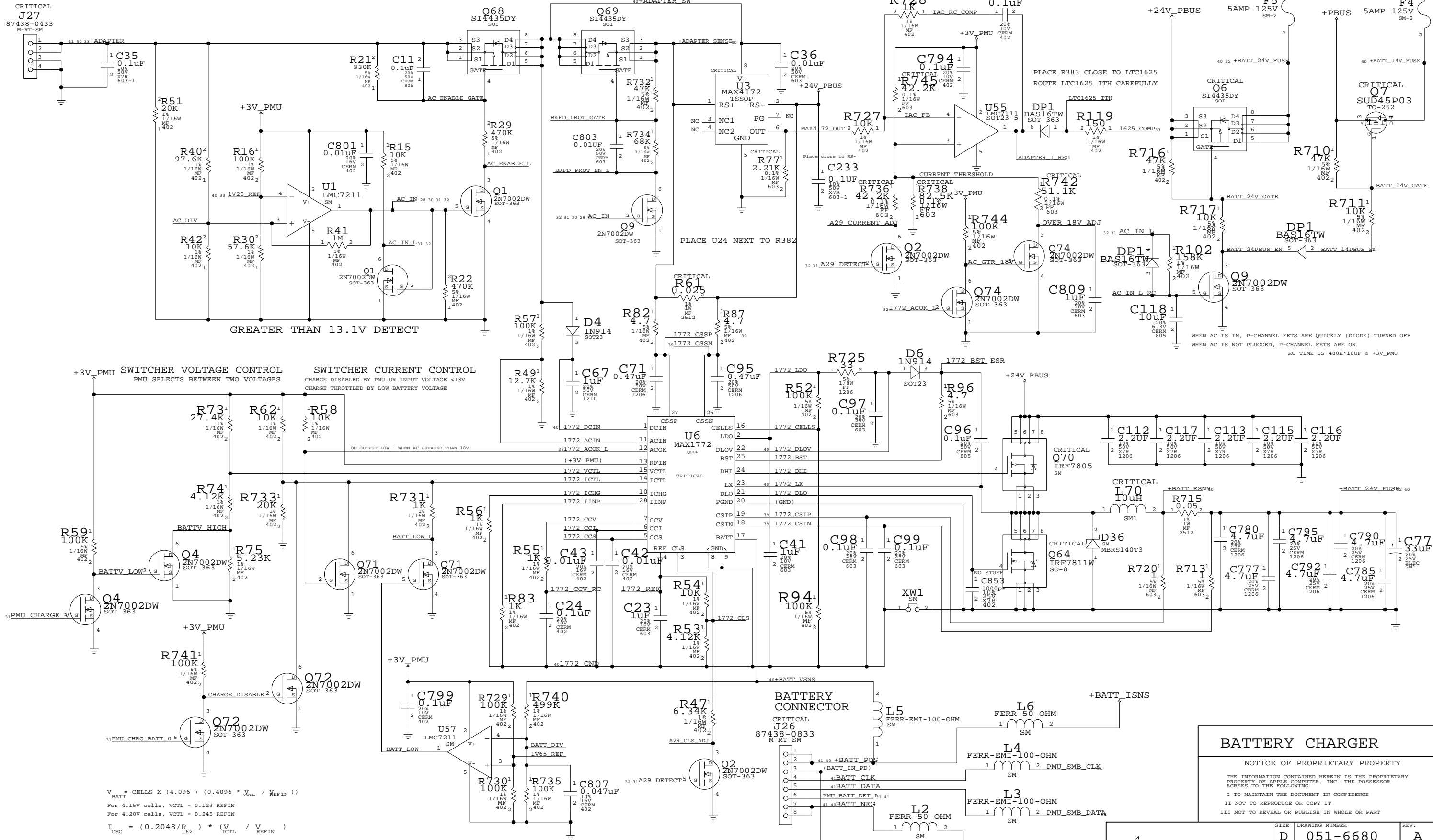
(POWER JACK, ETC. ON SEPARATE BOARD)

# DC INRUSH LIMITER

# BACKFEED PROTECTION

# +PBUS CURRENT LIMIT

# BATTERY SWITCH-OVER CIRCUIT



$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times \frac{V_{VCTL}}{V_{REFIN}}))$$
  
$$I_{CHG} = (0.2048 / R_{G2}) \times (\frac{V_{ICTL}}{V_{REFIN}})$$

# BATTERY CHARGER

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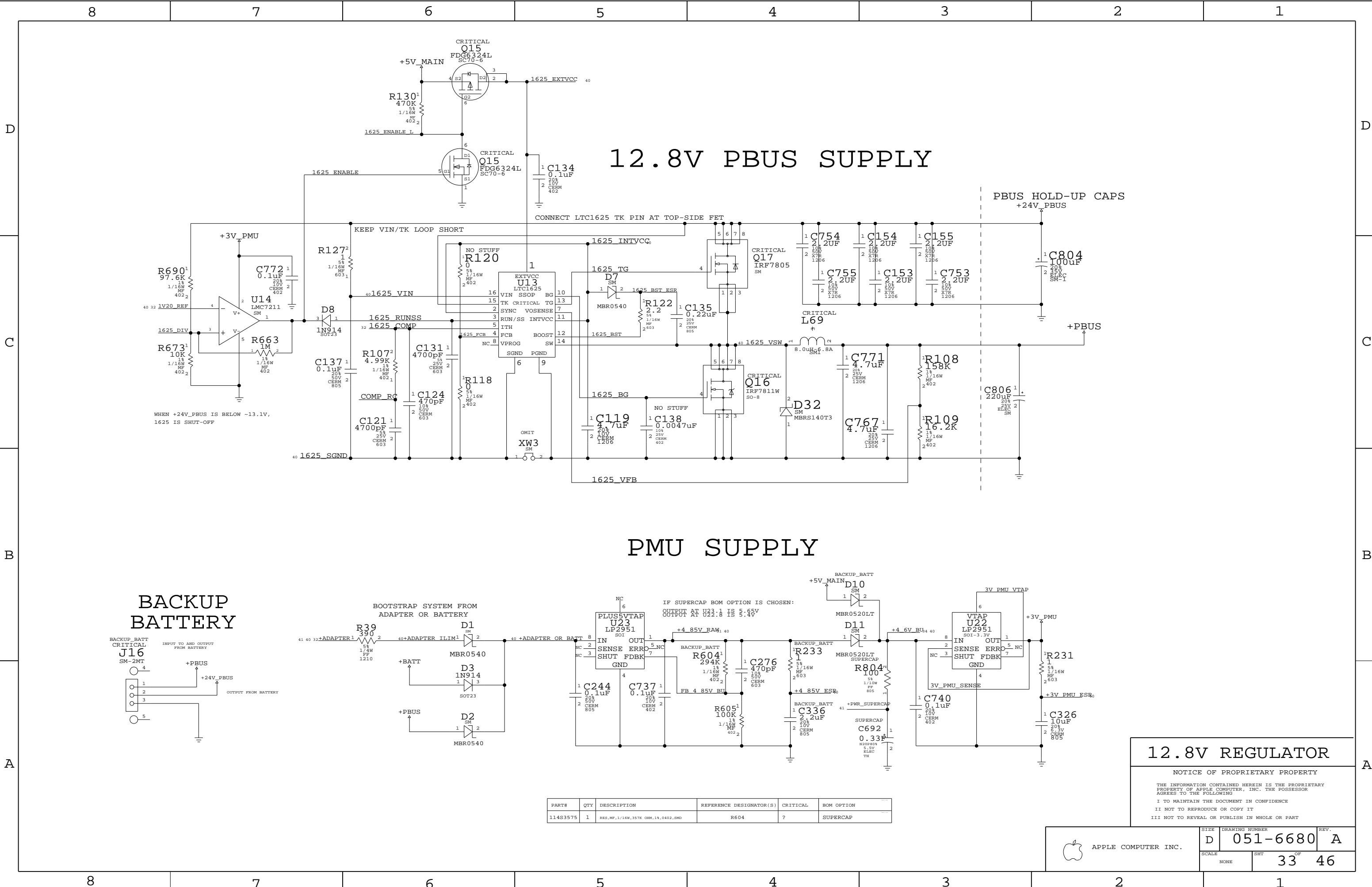
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SIZE	D	DRAWING NUMBER	051-6680	REV.	A
SCALE	NONE	SHT	OF	32	46





# 12.8V PBUS SUPPLY

# PMU SUPPLY

## BACKUP BATTERY

## 12.8V REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MP,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP

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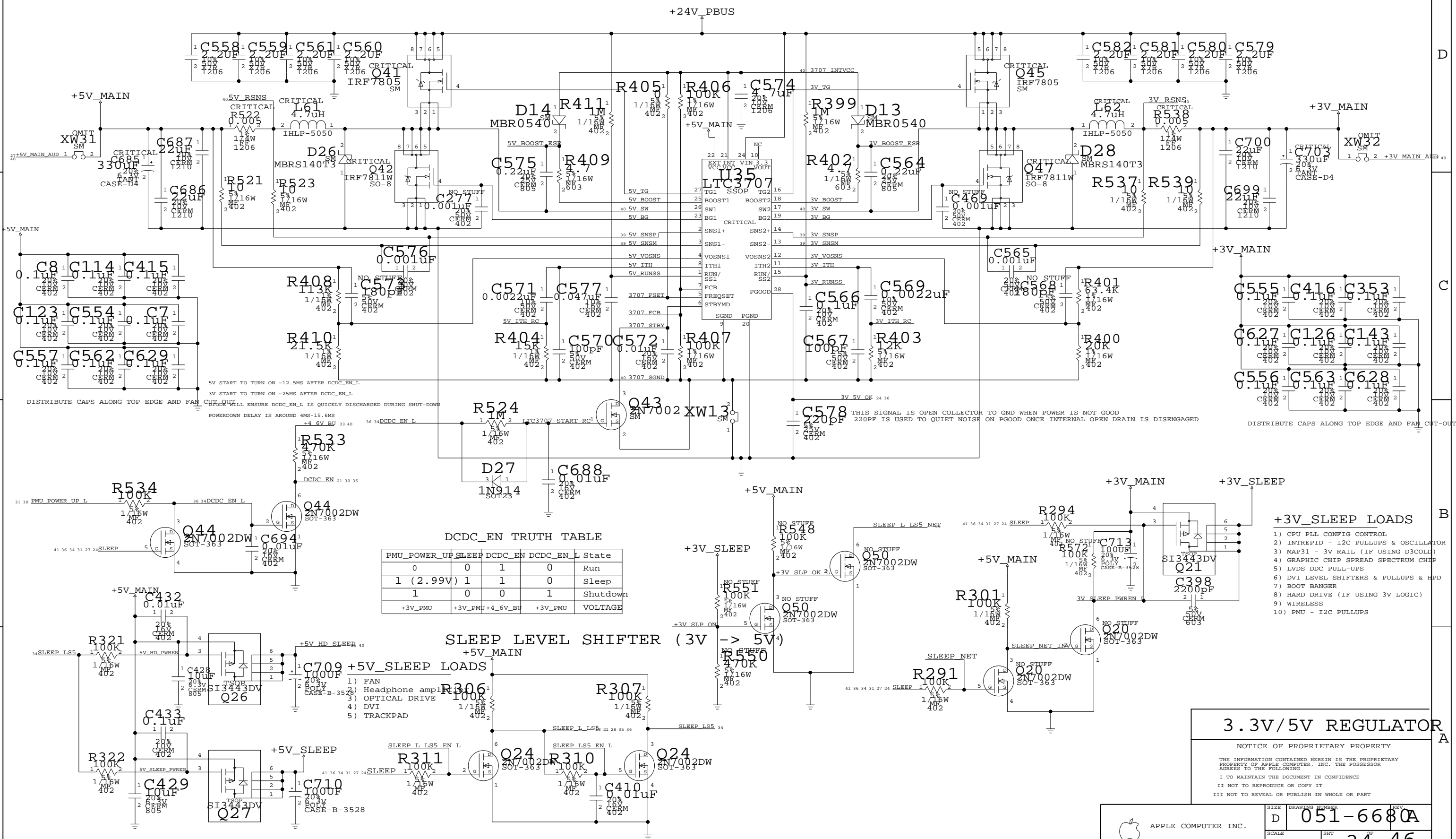
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

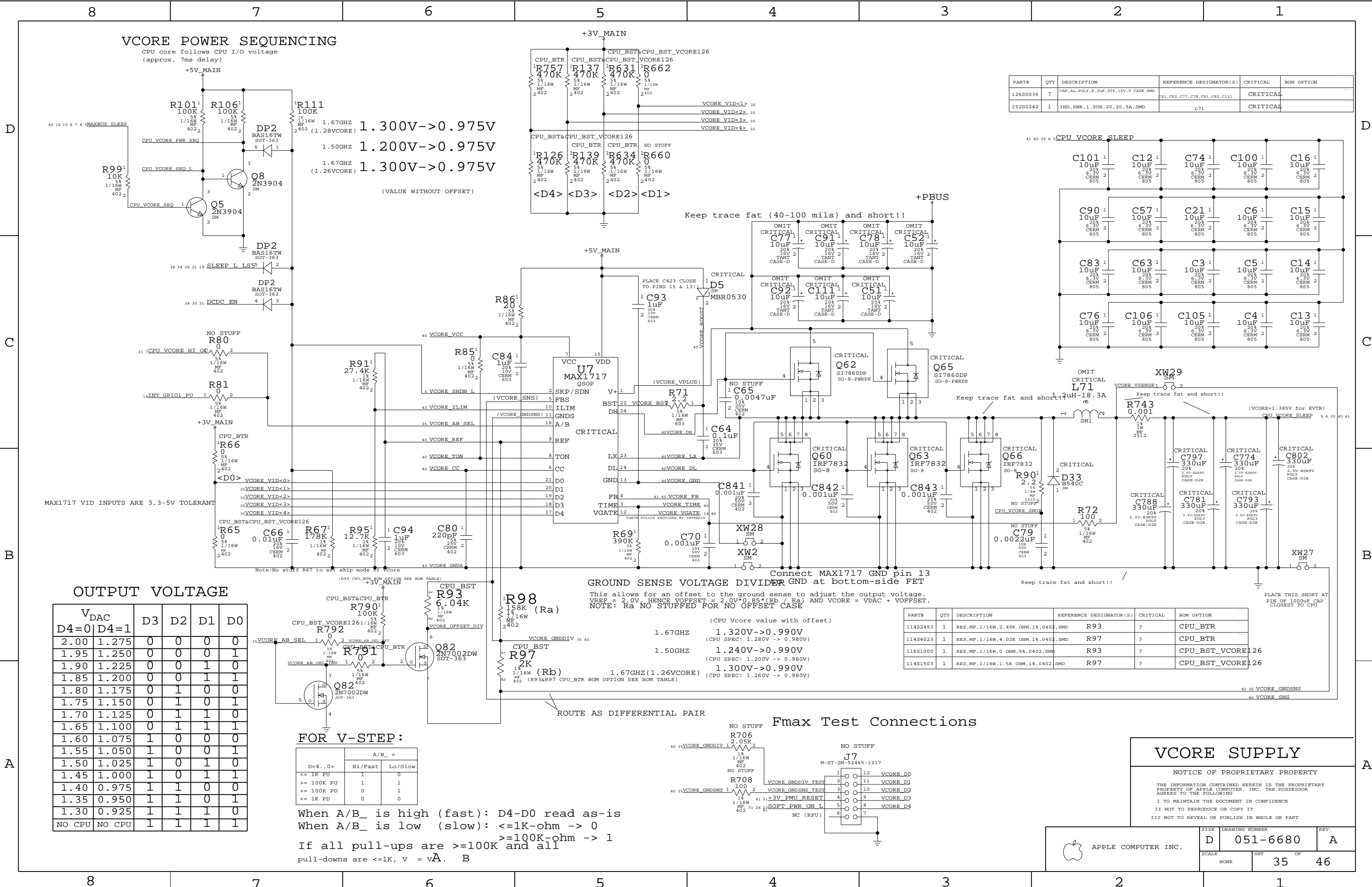
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	D	051-6680	A
SCALE		SHT	OF
NONE		33	46

# 3.3V/5V MAIN SUPPLY





VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage  
(approx. 7ms delay)

+5V\_MAIN

R100<sup>1</sup>  
100K  
1/16W  
MF  
402

R106<sup>1</sup>  
100K  
1/16W  
MF  
402

R111<sup>1</sup>  
100K  
1/16W  
MF  
402

1.300V->0.975V

1.50GHZ 1.200V->0.975V

1.67GHZ (1.26Vcore)

1.300V->0.975V

(VALUE WITHOUT OFFSET)

CPU\_VCORE\_PWR\_SEQ

CPU\_VCORE\_SEQ\_L

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

CPU\_VCORE\_SEQ

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CPU\_VCORE\_SEQ

OUTPUT VOLTAGE

V <sub>DAC</sub>		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B\_ is high (fast): D4-D0 read as-is

When A/B\_ is low (slow): <=1K-ohm -> 0

>=100K-ohm -> 1

If all pull-ups are >=100K and all

pull-downs are <=1K, v = vA. B

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.  
VREF = 2.0V, HENCE VOFFSET = 2.0V\*(Rb / Ra) AND Vcore = VDac + VOFFSET.  
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

	(CPU Vcore value with offset)
1.67GHZ	1.320V->0.990V (CPU SPEC: 1.280V -> 0.980V)
1.50GHZ	1.240V->0.990V (CPU SPEC: 1.200V -> 0.980V)
1.67GHZ(1.26Vcore)	1.300V->0.990V (CPU SPEC: 1.260V -> 0.980V)

Fmax Test Connections

VCORE SUPPLY

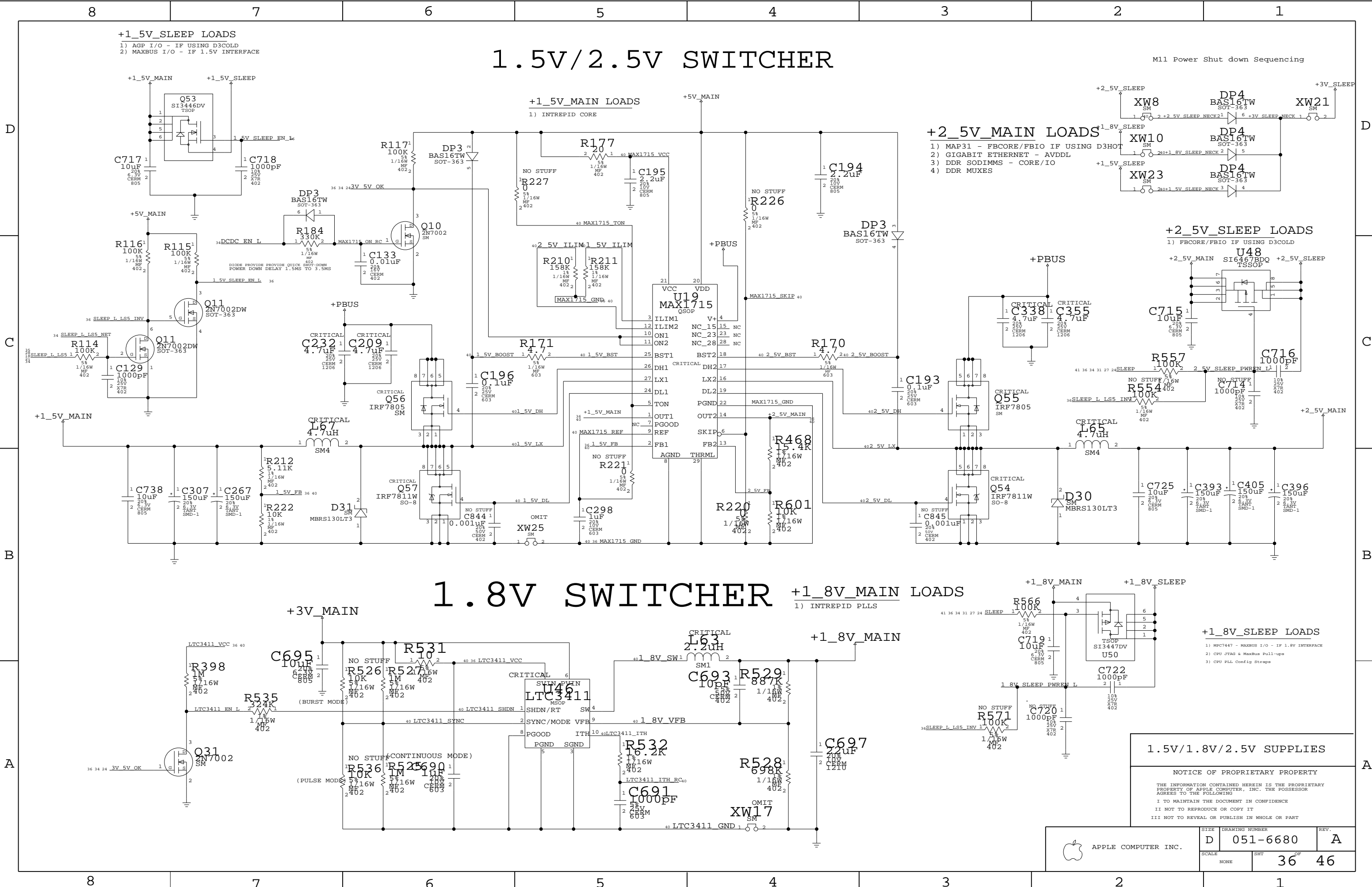
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SIZE	DRAWING NUMBER	REV.
D	051-6680	A
SCALE	SHT	OF
NONE	35	46



	8	7	6	5	4	3	2	1
DIGITAL SIGNALS	CLOCK LINE CONSTRAINTS							
	GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE_PARAM
	GROUP 0	MEM DATA<7..0>	L:S:1602:MIL:1700	7	500	(200)		167 MHZ
		MEM DOM<0>	L:S:1602:MIL:1700	MIL:7	500.0000	(200)		167.0 MHZ
		MEM DOS<0>	L:S:1602:MIL:1700	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<0>	L:S:1903:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS A<0>	L:S:1903:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA B<7..0>	L:S:2000:2100	7	500	(200)		167 MHZ
		RAM DOM B<0>	L:S:2000:MIL:2100	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS B<0>	L:S:2000:MIL:2100	MIL:7	500.0000	(200)		167.0 MHZ
	GROUP 1	MEM DATA<15..8>	L:S:1344:1660	7	500	(200)		167 MHZ
		MEM DOM<1>	L:S:1344:MIL:1660	MIL:7	500.0000	(200)		167.0 MHZ
		MEM DOS<1>	L:S:1344:MIL:1660	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<1>	L:S:1905:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS A<1>	L:S:1905:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA B<15..8>	L:S:2004:2412	7	500	(200)		167 MHZ
		RAM DOM B<1>	L:S:2004:MIL:2412	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS B<1>	L:S:2004:MIL:2412	MIL:7	500.0000	(200)		167.0 MHZ
	GROUP 2	MEM DATA<23..16>	L:S:1435:1500	7	500	(200)		167 MHZ
		MEM DOM<2>	L:S:1435:MIL:1500	MIL:7	500.0000	(200)		167.0 MHZ
		MEM DOS<2>	L:S:1435:MIL:1500	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<2>	L:S:1707:MIL:1800	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS A<2>	L:S:1707:MIL:1800	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA B<23..16>	L:S:1900:2000	7	500	(200)		167 MHZ
		RAM DOM B<2>	L:S:1900:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS B<2>	L:S:1900:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
	GROUP 3	MEM DATA<31..24>	L:S:1233:1485	7	500	(200)		167 MHZ
		MEM DOM<3>	L:S:1233:MIL:1485	MIL:7	500.0000	(200)		167.0 MHZ
		MEM DOS<3>	L:S:1233:MIL:1485	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<3>	L:S:1700:MIL:2165	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS A<3>	L:S:1700:MIL:2165	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA B<25..24>	L:S:1907:2356	7	500	(200)		167 MHZ
		RAM DATA B<26>	L:S:1907:MIL:2356	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA B<31..27>	L:S:1907:2356	7	500	(200)		167 MHZ
		RAM DOM B<3>	L:S:1907:MIL:2356	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS B<3>	L:S:1907:MIL:2356	MIL:7	500.0000	(200)		167.0 MHZ
	GROUP 4	MEM DATA<39..32>	L:S:1915:2000	7	500	(200)		167 MHZ
		MEM DOM<4>	L:S:1915:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		MEM DOS<4>	L:S:1915:MIL:2000	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DATA A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET	167 MHZ
		RAM DOM A<4>	L:S:1205:MIL:1387	MIL:7	500.0000	(200)		167.0 MHZ
		RAM DOS A<4>	L:S:1205:MIL:1387	MIL:7	500.0000	(200)		1

8		7		6		5		4		3		2		1		
DIGITAL SIGNALS	MAXBUS	GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	TEST	PULSE_PARAMS						
		CPU_AACK_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_ADDR<0..31>	L:S:1500:3100	7			(250)		TRUE	83 MHZ	5 8					
		CPU_ARTRY_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_BG_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_BR_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_CI_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_DATA<0..31>	L:S:1100:2700	7			(250)		TRUE	83 MHZ	6 8					
		CPU_DATA<32..63>	L:S:1100:2700	8			(250)			83 MHZ	6 8					
		CPU_DBG_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_DTI<0..2>	L:S:1500:2950	7			(250)				5 8					
		CPU_DRDY_L	L:S:1500 MIL:3200	MIL <sub>7</sub>			(250)				5 8					
		CPU_GBL_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_HIT_L	L:S:1500 MIL:2800	MIL <sub>7</sub>			(250)				5 8					
		CPU_QACK_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_OREQ_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_TA_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_TBST_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_TEA_L	L:S:1500 MIL:3000	MIL <sub>7</sub>			(250)				5 8					
		CPU_TS_L	L:S:1500 MIL:2700	MIL <sub>7</sub>			(250)				5 8					
		CPU_TSIZ<0..2>	L:S:1500:3500	7			(250)				5 8					
		CPU_TT<0..4>	L:S:1500:3400	7			(250)				5 8					
		CPU_WT_L	L:S:1500 MIL:3100	MIL <sub>7</sub>			(250)				5 8					
				STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2												



8	7	6	5	4	3	2	1
POWER NET CONSTRAINTS				SIGNAL CONSTRAINTS - PAGE 3			
D	MAIN/SLEEP	GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
			+24V PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+BATT	VOLTAGE=12.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=25	41
			+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+5V MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+5V SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+3V MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 41
			+3V SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
			+3V PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+2.5V MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
C	ADAPTER		+2.5V SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+1.8V MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
			+1.8V SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+1.5V MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+1.5V SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+1.5V LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+1.5V SLEEP VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
			+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33 41
			+ADAPTER SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
			+ADAPTER SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
B	BATTERY CHARGER		+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
			BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
			1772 DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
			1772 LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
			+BATT_14V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
			+BATT_24V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
			+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
			+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			1772 LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
			1772 DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
A	PMU		1772 GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
			+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
			+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
			+4.85V RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		33 33
			+4.6V BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		33 34
			+4.85V ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		33
			+3V PMU ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		33
			+3V PMU AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32 33
			+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 34
			+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	TRACKPAD		+5V_TP_AD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		41
			+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		24 41
			+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
			+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
			+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
			+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23 41
			+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23
			+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	23 41
			+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
			GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		23
	AUDIO						



# FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.  
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC\_QTY IS FOR REFERENCE AND  
LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.  
FUNC\_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG ASIC TMS	TRUE		13 28
	JTAG ASIC TDI	TRUE		13
	JTAG ASIC TDO_TP	TRUE		13
	JTAG ASIC TCK	TRUE		13 28
	JTAG ASIC TRST L	TRUE		13 28
	CPU CHKSTP_OUT L	TRUE		5
	CPU SRESET L	TRUE		5
	CPU HRESET L	TRUE		5 6 7
	JTAG CPU TMS	TRUE		5 6
	JTAG CPU TDI	TRUE		5 6
	JTAG CPU TDO_TP	TRUE		5
	JTAG CPU TCK	TRUE		5 6
	JTAG CPU TRST L	TRUE		5 6
	INT JTAG TEI	TRUE		13
	INT TST MONIN_PD	TRUE		13
	INT TST MONOUT_TP	TRUE		13
	INT TST_PLEN_PD	TRUE		13
	INT I2C_CLK0	TRUE		6 11 13 24
	INT I2C_DATA0	TRUE		6 11 13 24
	INT I2C_CLK1	TRUE		13 14 24 25 27
INT I2C	INT I2C_DATA1	TRUE		13 14 24 25 27
	+PBUS	TRUE		40
PWR/GND	+24V_PBUS	TRUE		40
	GPU_VCORE	TRUE		19 21 40
	1778_VFB	TRUE		21 40
	CPU_VCORE_SLEEP	TRUE		5 6 35 40
	VCORE_FB	TRUE		35 40
	+1_8V_MAIN	TRUE		40
	+2_5V_MAIN	TRUE		40
	+5V_MAIN	TRUE	2	40 41
	+5V_SLEEP	TRUE	2	40 41
	+3V_MAIN	TRUE	4	24 40
	+3V_PMU	TRUE		40
	CBUS_DET_1_L	TRUE		2000
CARDBUS DVI	CBUS_DET_2_L	TRUE		2000
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UF	TRUE		1000
	DVI_DDC_DATA_UF	TRUE		1000
	DVI_HPD_UF	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
		TRUE	2	2000
		TRUE	6	1000
LVDS	LVDS_L0N			1000
	LVDS_L0P			1000
	LVDS_L1N			1000
	LVDS_L1P			1000
	LVDS_L2N			1000
	LVDS_L2P			1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
INVERTER		TRUE	2	2000
		TRUE	6	1000
	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
	TV_C	TRUE		1000
	TV_Y	TRUE		2000
S-VIDEO	TV_COMP	TRUE		2000
	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
	INT_I2S0_SND_TO_DAC	TRUE		1000
LIO	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_HP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
	SND_HP_SENSE_L	TRUE		1000
	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	3000
	+3V_SLEEP	TRUE		2000
				40 41
				40 41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 27 39
	NEC_USB_DAP	TRUE		17 27 39
	NEC_USB_DBM	TRUE		17 27 39
	NEC_USB_DBP	TRUE		17 27 39
	BT_USB_DM	TRUE		14 27 39
	BT_USB_DP	TRUE		14 27 39
	USB_TP4D_N	TRUE		14 24 39
	USB_TP4D_P	TRUE		14 24 39
	NEC_RUSB_PPON	TRUE		17 27
	NEC_RUSB_OCI_UF	TRUE		17 27
	PCI_AD<0..31>	TRUE		1000
	PCI_FRAME_L	TRUE		1000
	PCI_TRDY_L	TRUE		1000
	PCI_IRDY_L	TRUE		1000
	PCI_DEVSEL_L	TRUE		1000
	PCI_STOP_L	TRUE		1000
	PCI_PAR	TRUE		1000
	AIRPORT_PCI_REQ_L	TRUE		1000
	AIRPORT_PCI_GNT_L	TRUE		1000
	AIRPORT_PCI_INT_L	TRUE		1000
RT. USB WIRELESS	MAIN_RESET_L	TRUE		1000
	CLK33M_AIRPORT	TRUE		1000
	PMU_PME_L	TRUE		1000
	ROM_ONBOARD_CS_L	TRUE		1000
	ROM_OE_L	TRUE		1000
	ROM_CS_L	TRUE		1000
	ROM_RW_L	TRUE		1000
	RF_DISABLE_L	TRUE		1000
	AIRPORT_CLKRUN_L	TRUE		1000
	+3V_AIRPORT	TRUE		2000
		TRUE	6	1000
				40
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000
	EIDE_OPTICAL_DMA_RQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CS1_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
	+5V_TP4D_SLEEP	TRUE		3000
TRACKPAD	TP4D_F_TXD	TRUE		3000
	TP4D_F_RXD	TRUE		3000
				40
				40
MODEM/SERIAL	SOFT_PWR_ON_L	TRUE		3000
	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
	COMM_TXD_L	TRUE		4000
	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
KEYBOARD	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
	KBD_X<0..9>	TRUE		3000
	KBD_Y<0..7>	TRUE		3000
	+BATT_POS	TRUE		1000
	BATT_NEG	TRUE		1000
BATTERY	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
	PMU_BATT_DET_L	TRUE		1000
				31 32
FANS	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
ETHERNET	FAN2_GND	TRUE		3000
	MDI_P<0..3>	TRUE		1000
	MDI_M<0..3>	TRUE		1000
				28 39
FIREWIRE	FW_TP00P	TRUE		1000
	FW_TP00N	TRUE		1000
	FW_TP00R	TRUE		1000
	FW_TP10P	TRUE		1000
	FW_TP10N	TRUE		1000
	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000
				41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TP01P	TRUE		1000
	FW_TP01N	TRUE		1000
	FW_TP11P	TRUE		1000
	FW_TP11N	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
				32 33 40
LMU/ALS	ST7_SLEEP_LED_H	TRUE		24
	PMU_SLEEP_LED	TRUE		24
	PMU_LID_CLOSED_L	TRUE		24 31
	LMU_DETECT	TRUE		24
MISC.		TRUE	6	1000
			(100 MIL PROBE PREFERRED)	40
	SLEEP_LED	TRUE		24
	PMU_KB_RESET_L	TRUE		24
	SLEEP	TRUE		24 27 31 34 36
	PMU_CPU_HRESET_L	TRUE		6 31
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		31 35
	MMM_ACC_X_AXIS	TRUE		25
	MMM_ACC_Y_AXIS	TRUE		25
	MMM_ACC_Z_AXIS	TRUE		25
	MMM_ACC_SELFTEST	TRUE		25
REMOVE CONSTRAIN FOR UNUSED FUNCTIONAL TP	+BATT_ISNS_P	TRUE		25
	+PPBATT_ISNS_N	TRUE		25
	+PWR_SUPERCAP	TRUE		33
	+3V_HALL_EFFECT			24 40
	LID_CLOSED_L			24
	TMDS_DN<0..2>			20 23 39
	TMDS_DP<0..2>			20 23 39
				20 23 39
				20 23 39
				20 23 39
				20 23 39
				20 23 39
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SCALE		NONE	SHT	OF
			41	46

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<div>REVISION HISTORY</div> <div>EVT2 RELEASE</div> <div>08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH 2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462) 3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2 4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT 5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING</div> <div>08/16/04 - 1. MODIFY CPU_AVDD SETTING</div> <div>08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT</div> <div>09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES</div> <div>09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN 2. MODIFY CPU_AVDD SEETING AGAIN 3. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM</div> <div>09/03/04 - 1. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802 2. ADD R803 BETWEEN DP6 AND DCDC_IN 3. ADD R804 AND SUPERCAP C692 ON +4_6V_BU 4. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT</div> <div>09/06/04 - 1. ADD EMI SOLUTION L12</div> <div>09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT</div> <div>09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT</div> <div>09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT</div> <div>09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT 2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU</div> <div>09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33 2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR</div> <div>DVT RELEASE</div> <div>09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT</div> <div>10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT</div> <div>10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR</div> <div>10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467</div> <div>11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313</div> <div>PVT RELEASE</div> <div>12/17/04 - 1. REMOVE ALL OPEN JUMPER</div> <div>12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION</div>							
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<div>SCALE</div> <div>NONE</div>		<div>SHT</div> <div>42</div>	<div>OF</div> <div>46</div>				
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